TELECOMMS INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors

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Bipolar

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Quality data

Plessey Semiconductors have an active **BS9300** and **BS9400** qualification approval programme on a number of products.
Additionally, Plessey Semiconductors are keen to co-operate in pursuing **BS9000** approval on any of the products which it manufactures.
For further information contact the Military Marketing Group at Swindon.

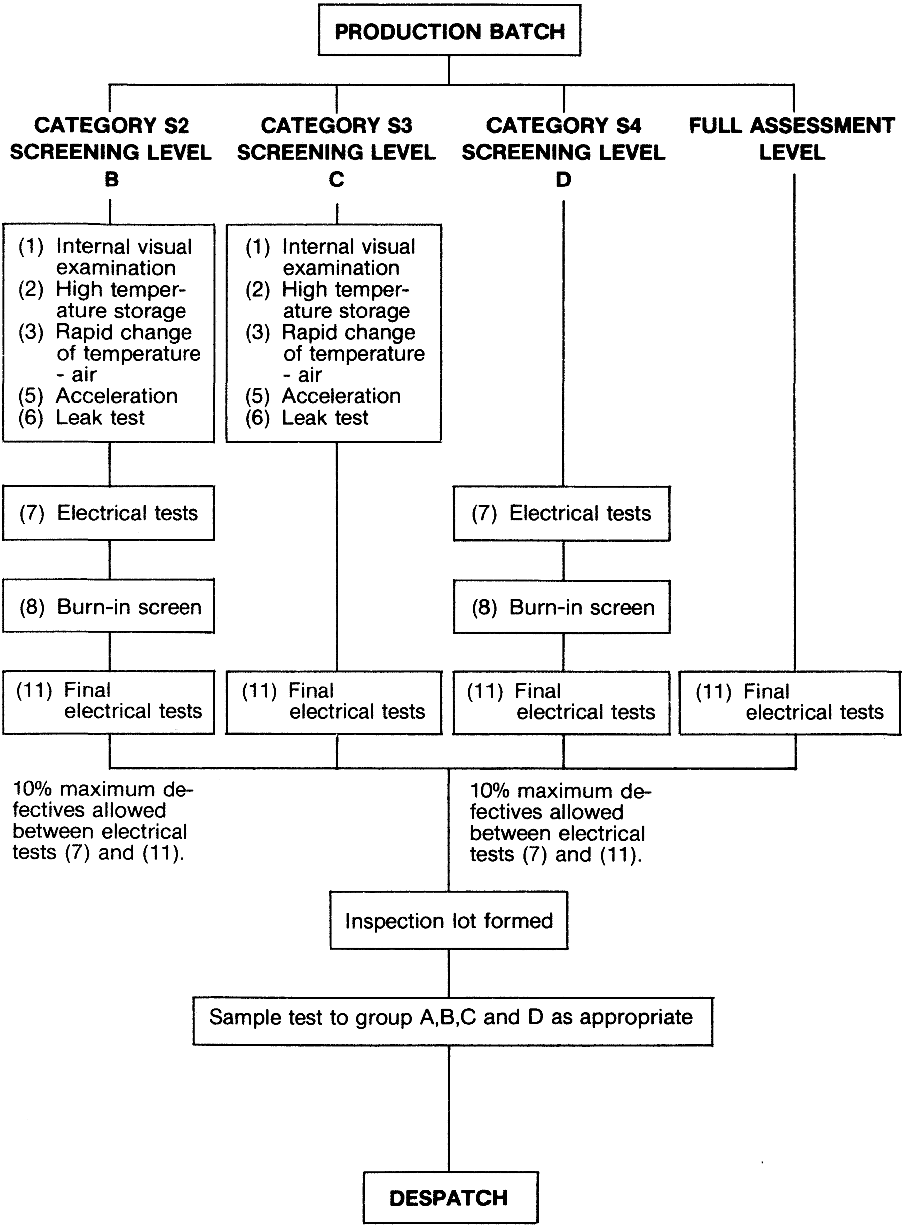
Plessey Semiconductors QA offers:

a) Factory Approval to
  BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)
  BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)
  CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers
  DEF STAN 05—21 QC System requirements for Industry (Equivalent to AQAP—1) Certificate 65752/1/01 refers

b) Additional Release Conditions to
  6/49 Defence Quality Assurance Board Certificate (DQAB 38020)
  MOD (N) Navy Department Inspection Authority
  or
  Private Sales Plessey's own Certificate of Conformance

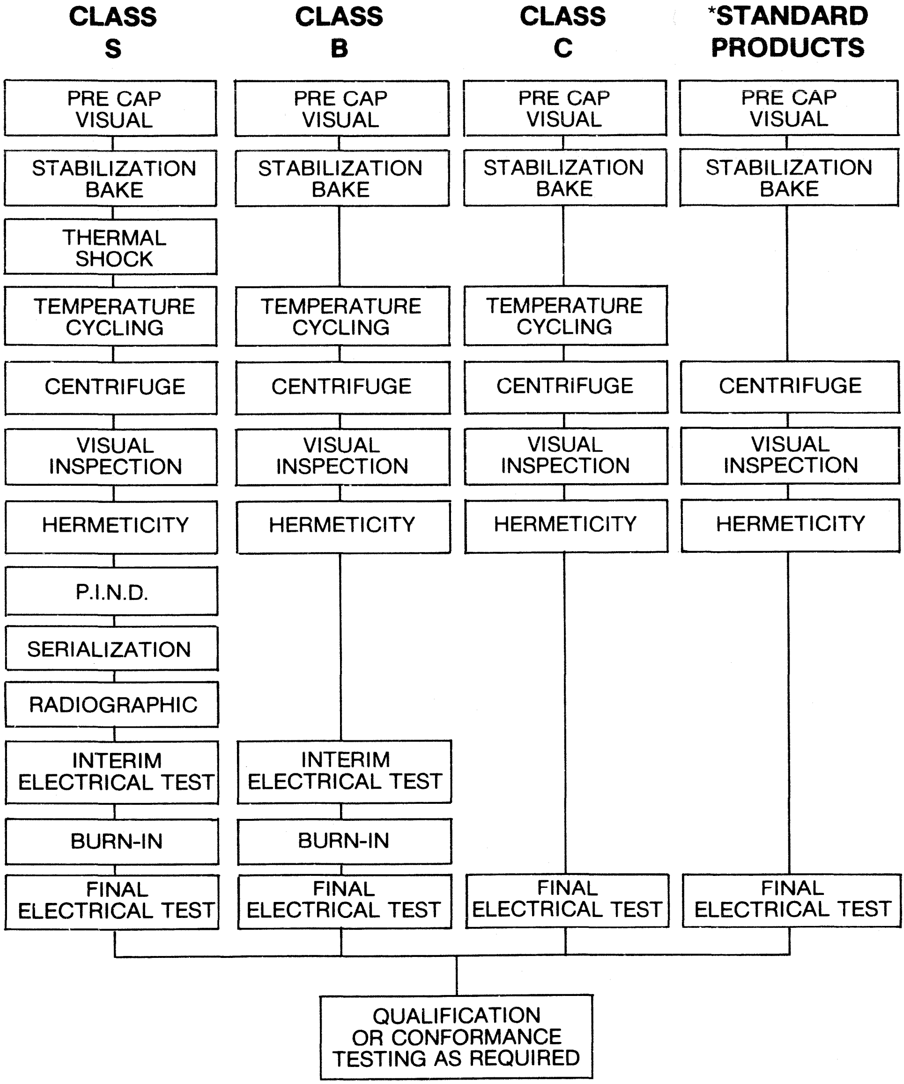
Devices are also manufactured, tested and supplied to **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

Screening to BS9400



Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

Semi-custom design techniques give users the advantages of integrated circuits dedicated to their applications without incurring the costs associated with full custom design. The techniques are particularly attractive to users with a low-to-moderate annual production potential of 1000 to 100,000 pieces, although these limits are flexible and may depend on the individual circuit. The economics of 'when to choose semi-custom' are illustrated in Fig.1.

Plessey Semiconductors offer semi-custom facilities in N-Channel MOS, CMOS and Bipolar technologies, using the techniques of Microcell, Gate Arrays and Analogue Arrays, the essential characteristics of which are detailed in Table 1.

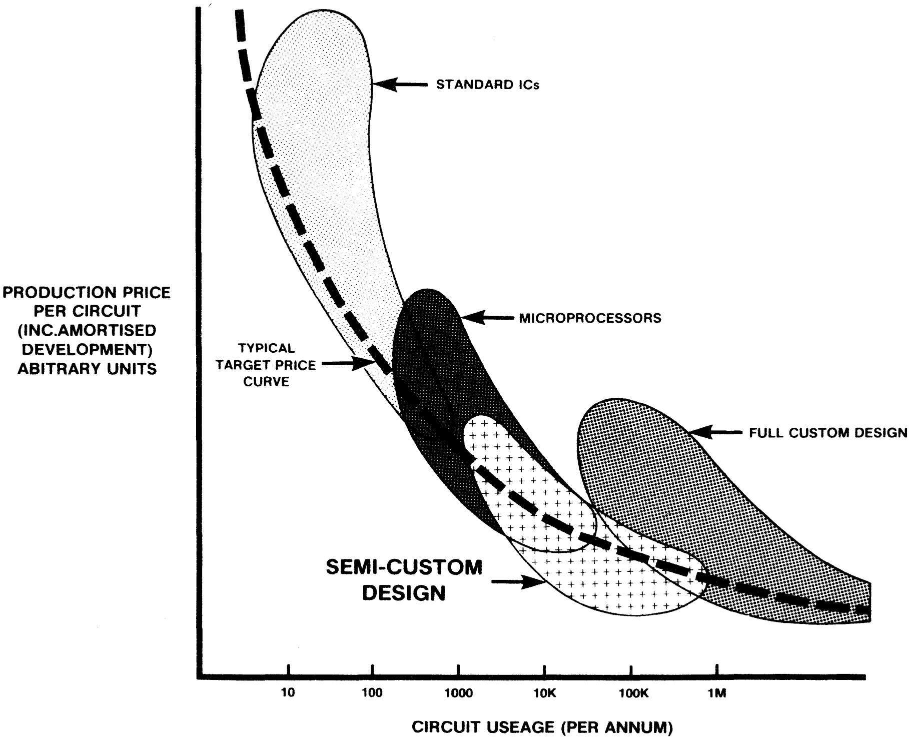


Fig 1 Areas of application of different categories of integrated circuits

MICROCELL

Microcell is a combination of standard cells with a formalised gate and interconnection procedure. It uses a computer library of gates and other cells which the designer calls up as required, leaving as much or as little space for interconnection as the design necessitates. Each circuit is exactly the right size for its function, and layout for the interconnection pattern is both straightforward and fast because of the error-correcting digitising technique employed.

The main features of Microcell can be summarised as follows: • From logic diagram to first samples in less than four months • Very high design integrity • A circuit can be produced by any competent logic designer • Minimal extra engineering effort is required • Clock rates of up to at least 2MHz are achievable • Advances in semiconductor technology and circuit design ideas can easily be absorbed into Microcell.

GATE ARRAYS

In the Gate Array, logic elements are pre-positioned and the customer's task is to design the interconnection of those elements (within the space allocated) to achieve the required functions. The cells are not necessarily committed to logic functions, but may in some cases be connected to form simple linear functions. Layout aids and software routines are normally used extensively to assist in the design, verification and testing of these structured devices.

Plessey Semiconductors offer Gate Array techniques in CMOS and ECL. CMOS Gate Arrays offer the following features: • High Speed ISO-CMOS Silicon Gate technology, giving a typical propagation delay of 6ns for a 2-input NAND gate (at 5V and 25°C) • Short turn round time • Inputs and outputs TTL and CMOS compatible and provided with static protection • On-chip power on reset option available • Available to commercial, industrial and military standards.

ECL Gate Arrays - also possessing the advantages of low development charge, increased reliability and fast delivery of samples - would be chosen mainly for the very high speed operating capability.

ANALOGUE ARRAYS

Plessey Semiconductors' Analogue Array brings Semi-Custom techniques to the designer of linear and other analogue circuits, for applications such as signal processing, amplification, waveform generation and function generation.

Manufactured on Bipolar Process I the analogue array features: • 159 NPN transistors (4 high current) • 58 PNP transistors • 385 resistors • 20V breakdown voltage • Functional compatibility with Exar and Interdesign • Single layer customisation on a grid system • Device library and simulation facilities.

Comprehensive technical literature on all Plessey Semiconductors' Semi-Custom Facilities is available on request.

SEMI-CUSTOM OPTION	TECHNOLOGY	SPEED	POWER CONSUMPTION	SCALE OF INTEGRATION	TYP. LEAD TIME TO 1ST SAMPLES
NMOS Microcell	NMOS Metal Gate	2MHz	300mW/1000 gates	500-2500 gates	16 weeks
Low Power NMOS Microcell	NMOS Metal Gate	0.5MHz	50mW/1000 gates	500-2000 gates	16 weeks
CMOS Microcell	ISO-CMOS	10MHz	0-150mW/1000 gates*	500-2000 gates	16 weeks
CMOS Gate Array	ISO-CMOS	8MHz	0-150mW/1000 gates*	560,960,1440 and 2014 gates	13 weeks
ECL Gate Array	Bipolar Process III	200MHz	75 gates: 900mW max 300 gates: 3.5W max	75 to 600 gates	14 weeks
Bipolar Analogue Array	Bipolar Process I	f_T = 500MHz	100mW to 1W**	217 transistors	16 weeks

* Depending on speed

** Depending on application

Table 1

Technical Data

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ADVANCE INFORMATION

MJ1410

8 BIT FORMAT CONVERTER

The MJ1410 is realised in N-channel MOS technology and operates from a single 5V supply. The circuit can be clocked from d.c. up to 2.5MHz and has 3-state output buffers capable of driving two LSTTL loads. All inputs are TTL compatible.

The MJ1410 performs the complementary functions of serial-to-parallel and parallel-to-serial data conversion on 8 bits of data. Both these conversions are achieved using the same time-position matrix, which has eight inputs and eight outputs.

An 8-bit parallel word clocked into the eight inputs appears as a serial 8-bit data stream on one of the eight outputs. Successive parallel words at the inputs appear as serial data streams on each of the eight outputs in turn.

Conversely, a serial 8-bit data stream on one of the eight inputs appears as an 8-bit parallel word on the eight outputs. Successive parallel words appearing at the eight outputs correspond to the serial data on each of the eight inputs in rotation.

The conversion can be 'programmed' to start in any register by setting the appropriate binary value on the counter pre-load inputs and applying a pulse to the Sync input. If the loading sequence produced by the counter is not required it can be disabled by connecting 'clock' to 'sync'. At each positive clock edge the register loaded will depend on the data on the counter inputs on the previous positive clock edge.

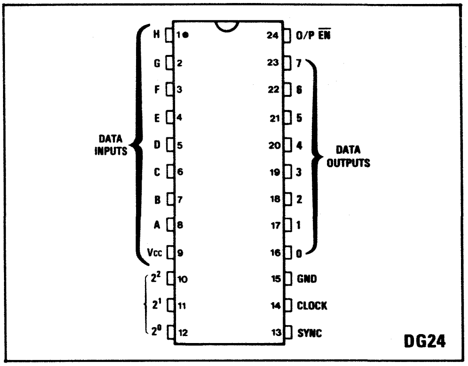

Fig.1 Pin connections

FEATURES

- Single 5V supply.
- Three-state outputs.
- All inputs TTL compatible.

FUNCTIONAL DESCRIPTION

Pin No.	Title	Function
1	H Data inputs	Data i/p H See Figs. 3 and 4
2	G	Data i/p G
3	F	Data i/p F
4	E	Data i/p E
5	D	Data i/p D
6	C	Data i/p C
7	B	Data i/p B
8	A	Data i/p A
9	Vcc	Positive supply, 5V ± 5%
10	2^2	Counter preset i/p bit 2 The counter is preset to the data on these i/ps on the 3rd positive clock edge following a negative edge on the 'sync' input.
11	2^1	Counter preset i/p bit 1
12	2^0	Counter preset i/p bit 0
13	SYNC	A negative edge on this i/p initiates the counter preset sequence which causes the conversion cycle to start in the register which corresponds to the binary value of the counter preset i/ps.
14	CLOCK	System clock
15	GND	Zero volts
16	0 Data outputs	Three state data o/p '0' See Figs. 3 and 4
17	1	Three state data o/p '1'
18	2	Three state data o/p '2'
19	3	Three state data o/p '3'
20	4	Three state data o/p '4'
21	5	Three state data o/p '5'
22	6	Three state data o/p '6'
23	7	Three state data o/p '7'
24	O/P $\overline{\text{EN}}$	A logic '1' on this i/p forces all the data outputs to a high impedance state.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{CC} = 5V, T_{amb} = 22°C ± 2°C, Test circuit: Fig. 6.
Supply voltage V_{CC} 5V ± 10%
Ambient operating temperature T_{amb} -10°C to +70°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level I/P voltage	V_{IL}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	-0.3		0.8	Volts	
High level I/P voltage	V_{IH}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	2.5		V_{CC}	Volts	
Low level I/P current/high level I/P current	I_{IN}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24		1	50	µA	
Low level O/P voltage	V_{OL}	16,17,18, 19,20,21, 22,23			0.5	Volts	I_{SYNC} = 1.6mA
High level O/P voltage	V_{OH}	16,17,18, 19,20,21, 22,23	2.5			Volts	I_{SOURCE} = 100uA
Low level O/P current sync capability	I_{OL}	16,17,18, 19,20,21, 22,23	-1.6			mA	
High level O/P current source capability	I_{OH}	16,17,18, 19,20,21, 22,23	100			µA	
OFF state O/P current	$I_{OFF\ L}$	16,17,18, 19,20,21, 22,23			40	µA	V_{OUT} = GND
	$I_{OFF\ H}$	16,17,18, 19,20,21, 22,23			-40	µA	V_{OUT} = V_{CC}
Power dissipation	P_{DISS}		90		500	mW	V_{CC} = 5.5V

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.clock frequency	$F_{max.}$	2.4		10	MHz	
Min. clock frequency	$F_{min.}$	0			MHz	
Sync. pulse width (positive)	t_{SPP}	60			ns	Fig. 6
Sync. pulse width (negative)	t_{SPN}	100			ns	Fig. 6
Lead of sync. clocking edge on positive clock edge	t_{SL}	130			ns	Fig. 6
Set up time of counter inputs ($2^0,2^1,2^2$)	t_{SC}	70			ns	Fig. 6
Hold time of counter inputs	t_{HC}	60			ns	Fig. 6
Set up time of data inputs (A-H)	t_{SD}	80			ns	Fig. 6

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Hold time of data inputs	t_{HD}	85			ns	Fig. 6
Propagation delay, data out valid from output $\overline{\text{ENABLE}}$ low	t_{PDE}			100	ns	Fig. 6
Propagation delay, data out disabled from output $\overline{\text{ENABLE}}$ high	t_{PDD}			100	ns	Fig. 6
Propagation delay, clock to data out valid	t_{PCD}			200	ns	Fig. 6

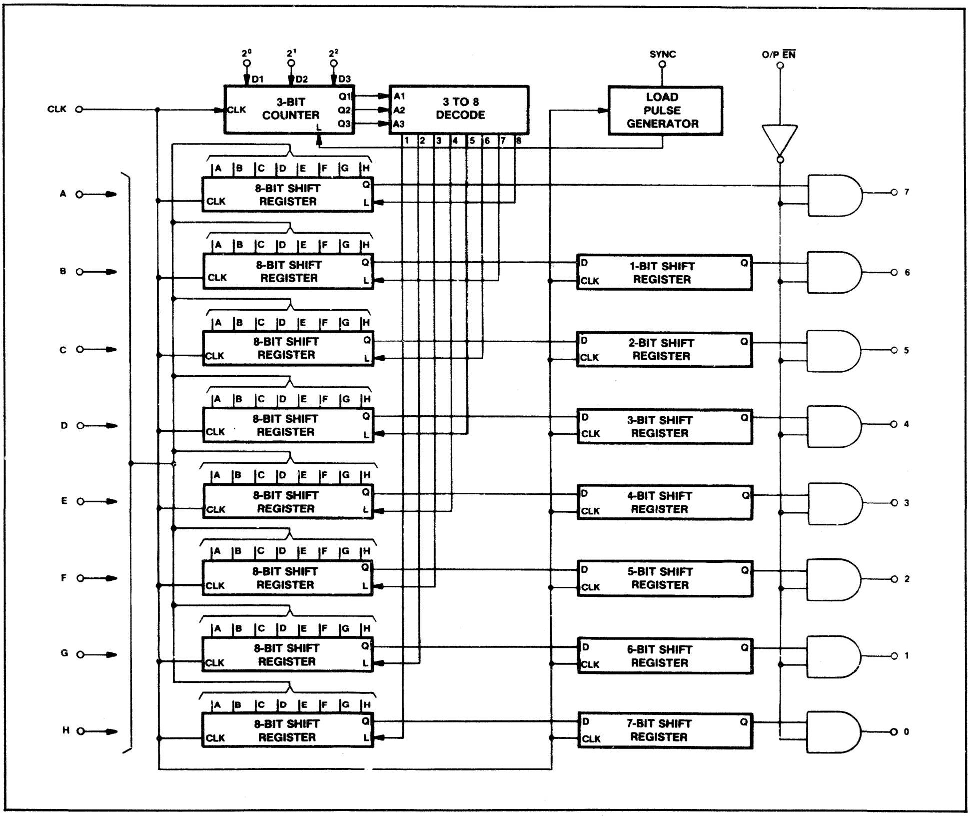

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. ground = 7V max.
Storage temperature = -55°C to +125°C

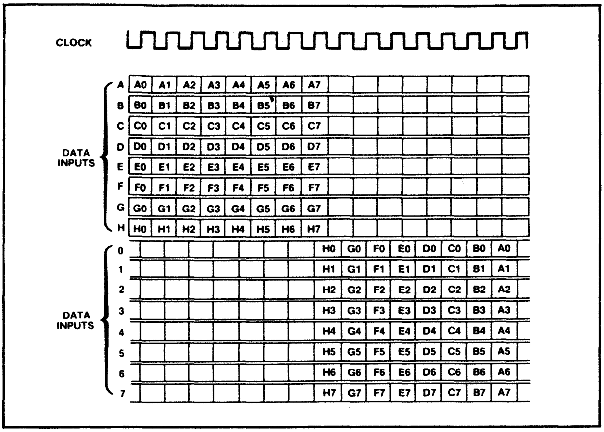

Fig.3 Data conversion

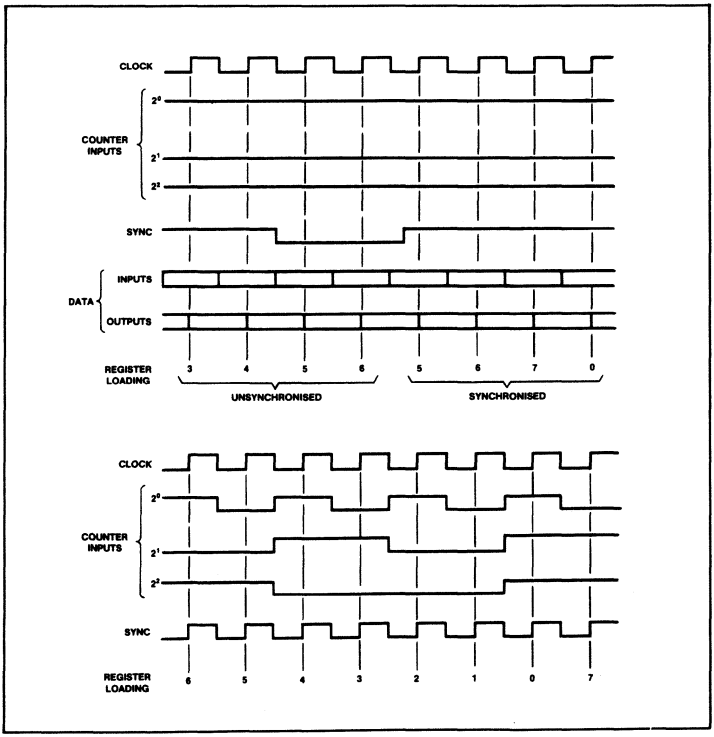

Fig.4 Input and output waveforms

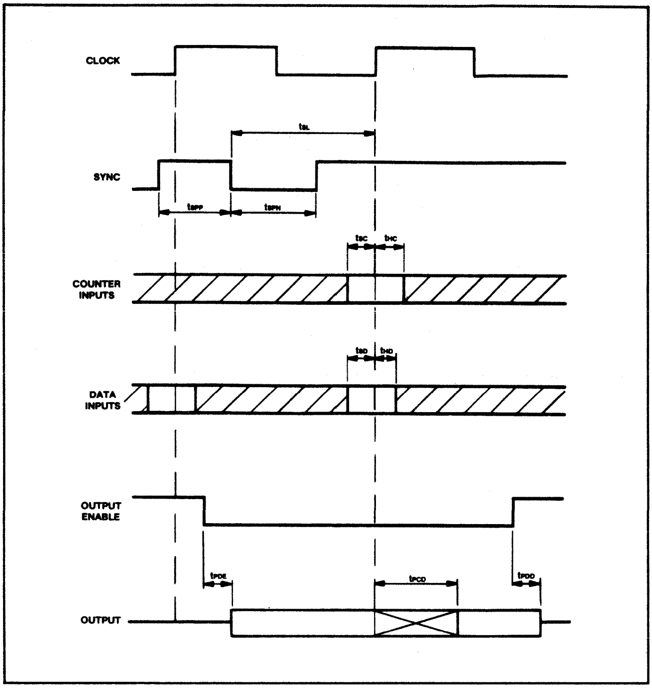

Fig.5 Timing details

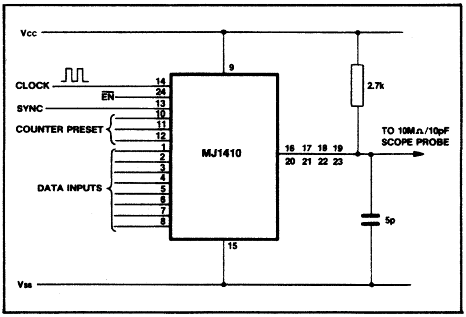

Fig.6 Test conditions

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2 MBIT PCM SIGNALLING CIRCUIT
MJ1440
HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

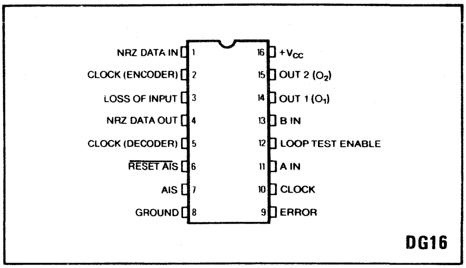

Fig. 1 Pin connections

FEATURES

- 5v ± 5% Supply − 50mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

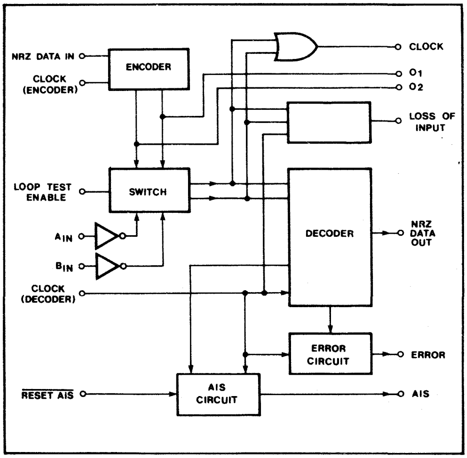

Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
40°C/Watt	120°C/Watt

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = 0°C$ to $+70°C$

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,5,6 10,11,12,13	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	μA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 80μA
		3,4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	3,4,7,9	2.7			V	Isource = 60μA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	50	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs.10, 15
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs.11, 15
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.10, 15. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10, 15
tpd1A-tpd1B				20	ns	Figs.10, 15
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = Figs.13, 15
Setup time of NRZ data in to Clock (Encoder)	ts3	75			ns	Figs.8, 10, 15
Hold time of NRZ data in	th3	55			ns	Figs.10, 15
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.9, 13, 15
Propagation delay Clock (Decoder) to loss of input				150	ns	
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.12, 15
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.14, 15
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.9, 11, 15. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.9, 11, 15
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.9, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	30			ns	Figs.9, 14, 15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	100			ns	Figs.9, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.14, 15

NOTES
1. Encoded HDB3 outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3)
2. The decoded NRZ output is delayed by 4 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4)

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ Data in
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1

3. Loss of input alarm
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'.

4. NRZ data out
Decoded data in NRZ form from ternary HDB3 input data (A_{in},B_{in}), data is clocked out by positive going edge of clock (Decoder).

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period.

Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts

9. Error
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

10. Clock
'OR' function of $\overline{A_{in}}$,$\overline{B_{in}}$ for clock regeneration when pin 12 = '0', 'OR' function of O_1,O_2 when pin 12 = '1'.

11,13. A_{in},B_{in}
Inputs representing the received ternary HDB3 PCM signal. A_{in} = '0' represents a positive going '1', B_{in} = '0' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the Clock (Decoder). A_{in} and B_{in} may be interchanged.

12. Loop test enable
Input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' O_1 is connected internally to A_{in}. O_2 is connected internally to B_{in}. Clock becomes the OR function $O_1 + O_2$. The delay from NRZ in to NRZ out is 7½ clock periods in the loop back condition.

14, 15. O_1, O_2
Outputs representing the ternary encoded data for line transmission O_1= '1' representing a positive going '1', O_2= '1' represents a negative going '1'. O_1 and O_2 may be interchanged.

16. V_{cc}
Positive supply, 5V ± 5%

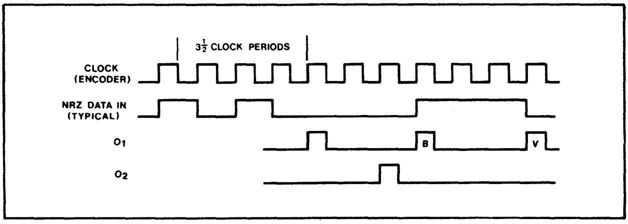

Fig. 3 Encode waveforms

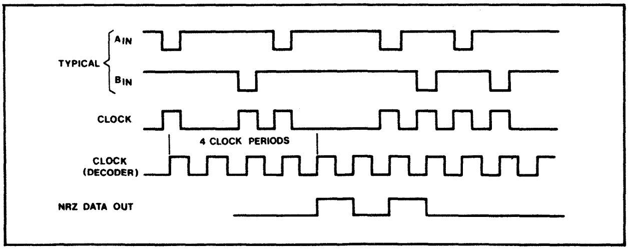

Fig. 4 Decode waveforms

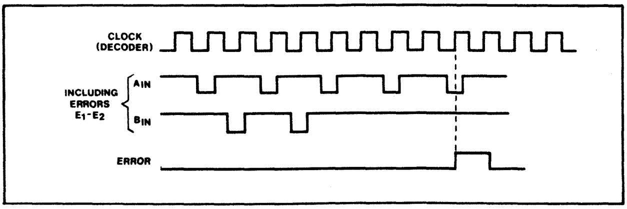

Fig. 5 HDB3 error output waveforms

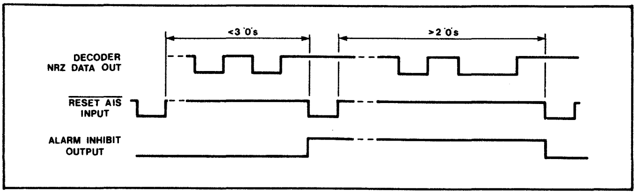

Fig. 6 AIS error and reset waveforms

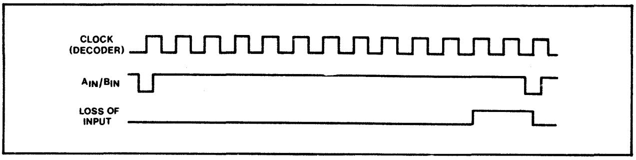

Fig. 7 Loss of input waveforms

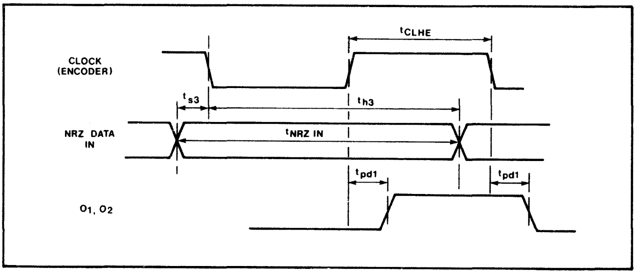

Fig. 8 Encoder timing relationship

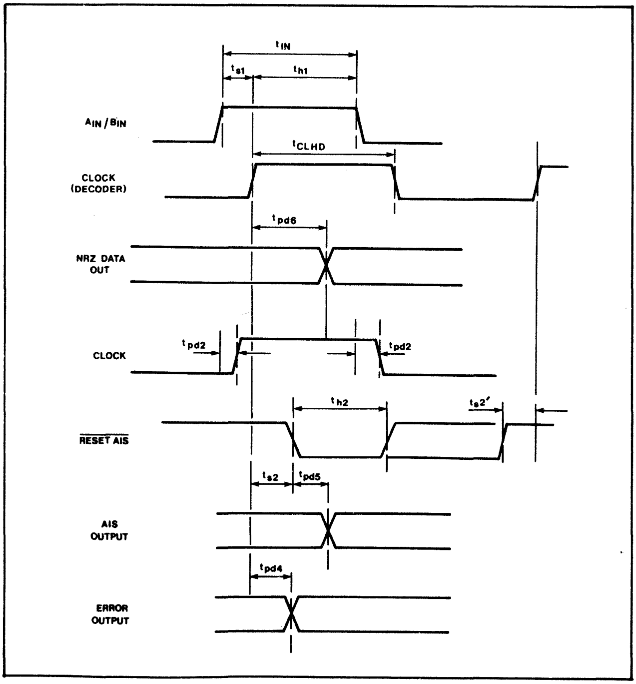

Fig. 9 Decoder timing relationship

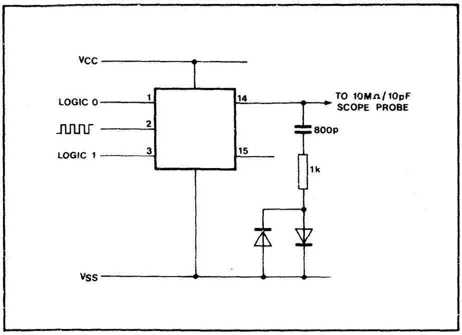

Fig. 10

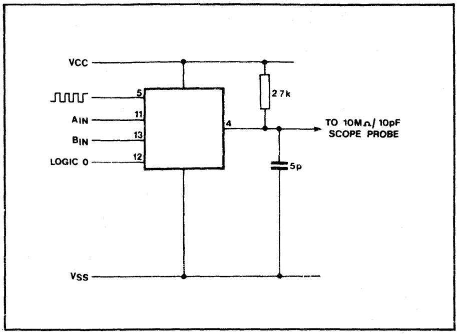

Fig. 11

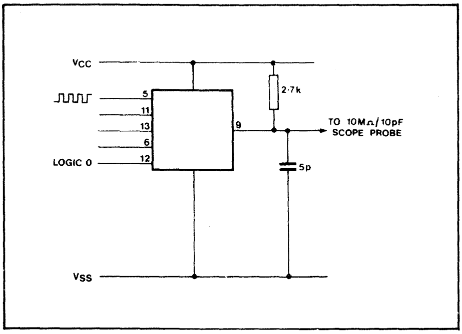

Fig. 12

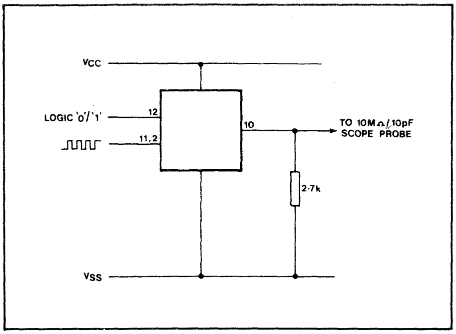

Fig. 13

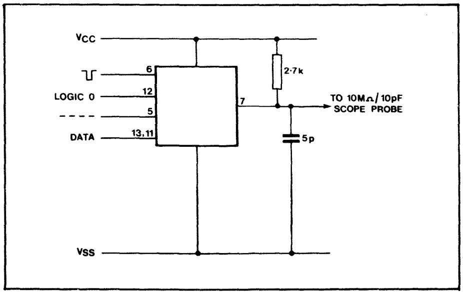

Fig. 14

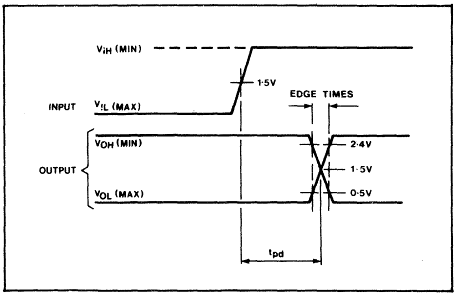

Fig. 15 Test timing definitions

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

PLESSEY Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{\text{SF}}$', and time slot 16 'TS16' outputs.

FEATURES

- 5V ±5% Supply—20mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

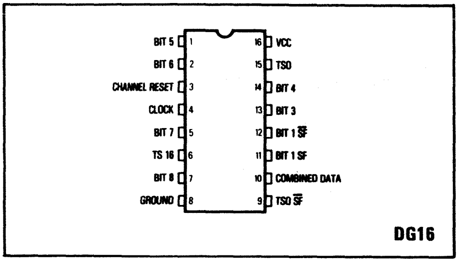

Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

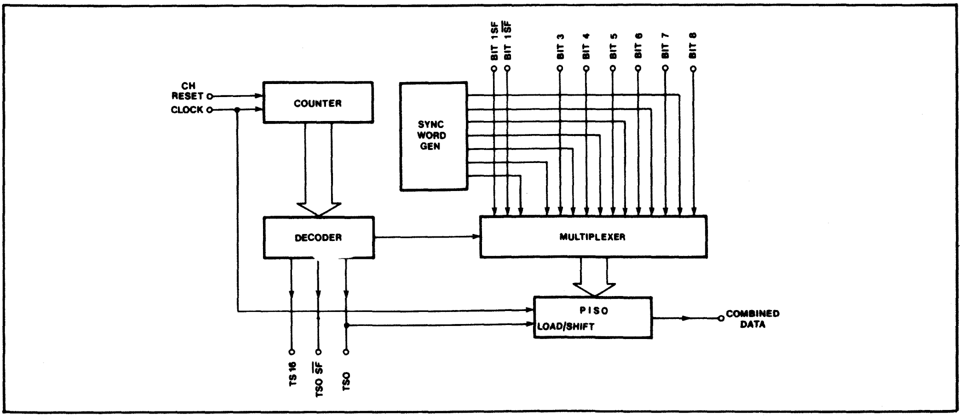

Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature - 10°C to + 70°C

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15 10			0.5 0.7	V V	$I_{sink} = 2mA$ $I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3	5		MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_P	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048 MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

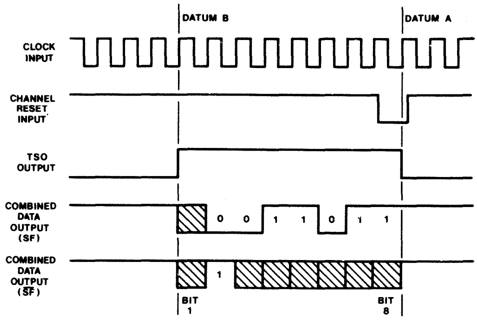

Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8

Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset

A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock

System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16

This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND

Zero volts.

9. TS0 $\overline{SF}$

This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data

This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X—indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$

Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0

This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}

Positive supply, 5V ±5%.

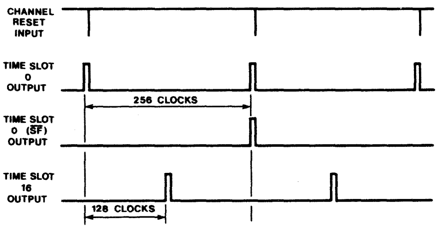

Fig.4 Sync. timing

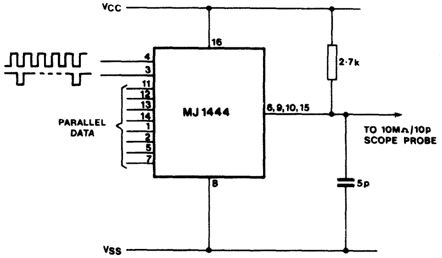

Fig.5 Test conditions (all outputs)

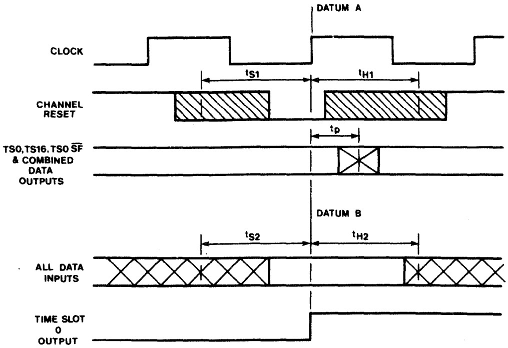

Fig.6 Timing definitions

PLESSEY
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PCM SYNCHRONISING WORD RECEIVER

MJ1445

2 MBIT PCM SIGNALLING CIRCUIT

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synchronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

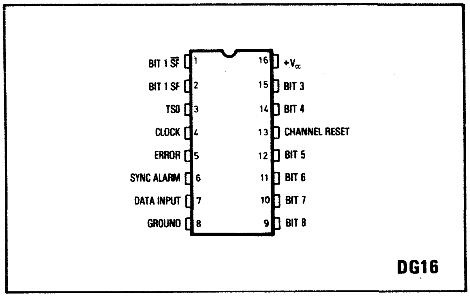


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply - 20mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance:	Chip to Case	Chip to Amb.
	35°C/Watt	120°C/Watt

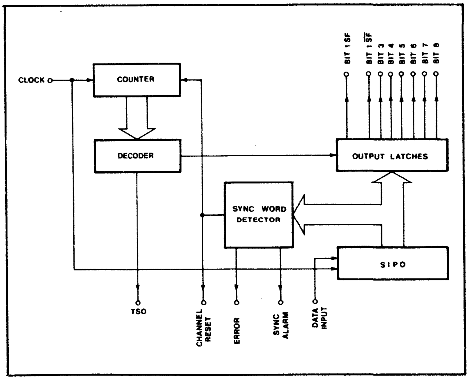


Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock frequency	f_{max}	2.2	4.5		MHz	
Input delay of data input	$t_{d\,data}$	20		200	ns	$f_{clock} = 2.048\,MHz$
Propagation delay, clock to TS0 output	$t_{d\,TS0}$	80		200	ns	Fig.3
Propagation delay clock to error output, sync alarm, spare bits and CH. Reset output high	t_d	50		400	ns	Fig.3
Propagation delay, clock to CH. Reset output Low $(T-t_p)$	t_p	100		450	ns	Fig.3

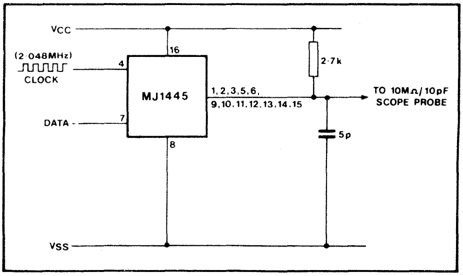


Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$

This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true at the end of the first bit of time slot 1.

2. Bit 1 SF

This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true at the end of the first bit of time slot 1.

3. TS0

This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock

System clock input (2.048MHz for a 2MBit PCM system).

5. Error

This output goes high at the end of time slot 0 in the 3rd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained.

6. Sync Alarm

This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data Input

Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND

Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8

These parallel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true at the end of the first bit of time slot 1.

13. Channel reset

This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}

Positive supply 5V ±5%.

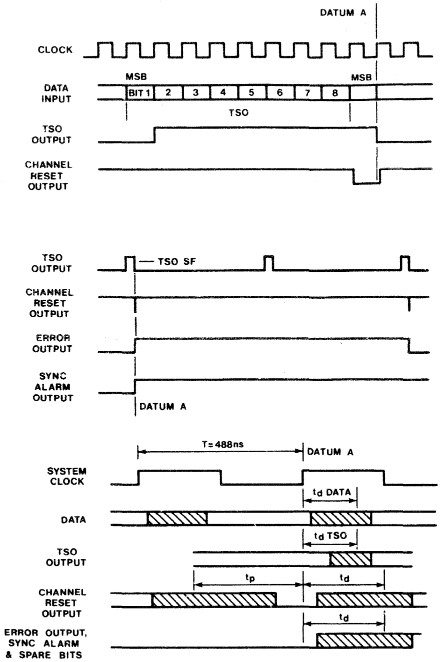


Fig.4 Timing diagram and output waveforms

2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

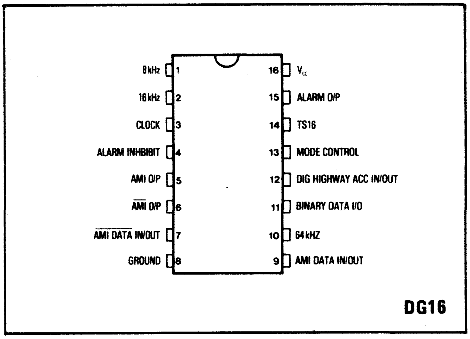


Fig.1 Pin connections

FEATURES

- 5V ±5% Supply—20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

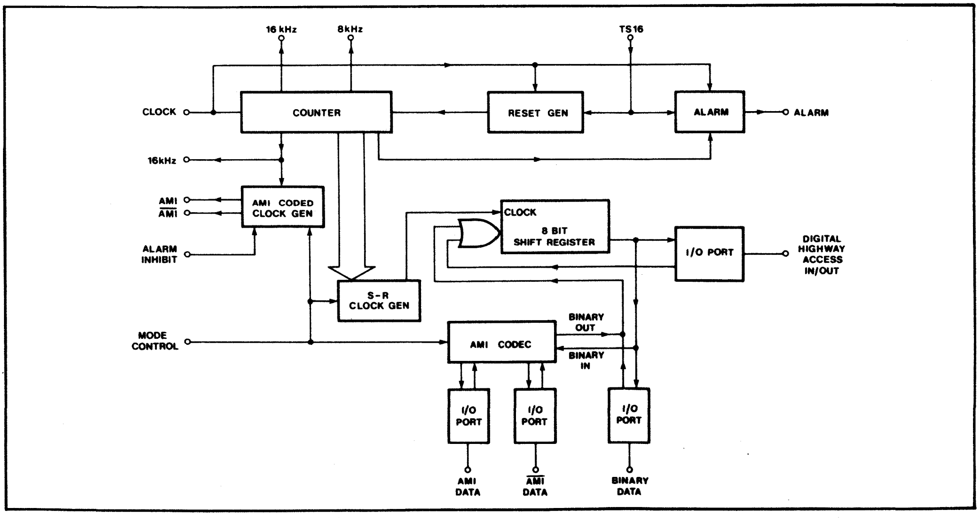


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	$I_{sink} = 2mA$
		12			0.5	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	$V_{CC} = 5.25V$

Dynamic Characteristics ($f_{clock} = 2.048MHz$)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\ DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\ TS16}$	80		200	ns	
Output delay 64kHz to 16kHz output	$t_{p\ 16}$			70	ns	Fig.7
Output delay, 64kHz to 8kHz output	$t_{p\ 8}$			170	ns	Fig.7
Output delay, 64kHz to binary data output (64kHz)	$t_{p\ BIN}$	20		450	ns	Fig.8
Output delay 64kHz to AMI, $\overline{\text{AMI}}$, AMI data & $\overline{\text{AMI}}$ data o/p's	$t_{p\ AMI}$	20		400	ns	Fig.8
Input delay, 64kHz to binary data in (64kHz)	$t_{d\ BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8kHz
8kHz square wave output.

2. 16kHz
16kHz square wave output.

3. Clock
System clock input (2.048MHz for a 2Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64kHz.

6. $\overline{\text{AMI}}$ output

7. $\overline{\text{AMI}}$ Data In/out
In the transmit mode 64kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data In/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64kbits/sec in AMI format.

10. 64kHz
64kHz square wave output.

11. Binary data in/out
In the transmit mode 64k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64kbits/sec in binary format.

12. Digital Highway access In/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply 5V ±5%.

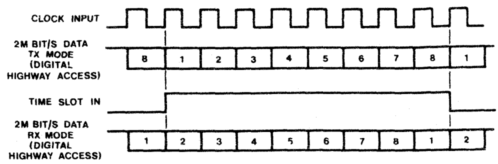


Fig.3 | 2MBit/s operation

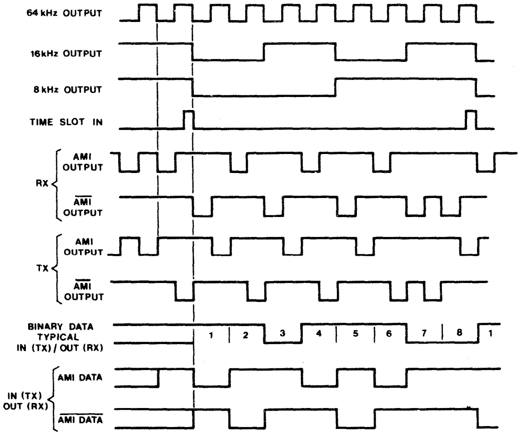


Fig.4 64kBit/s operation

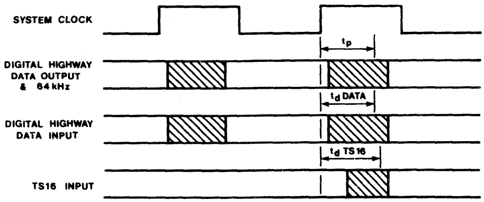


Fig.5 | Timing diagram

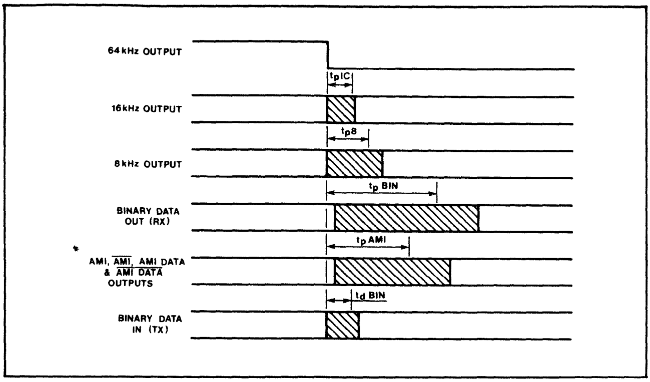


Fig.6 Timing diagram

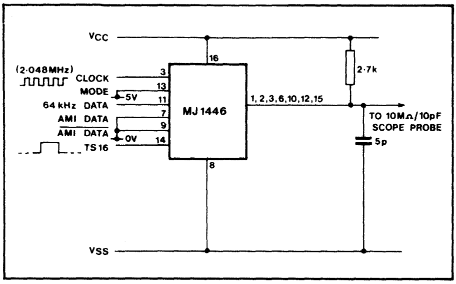


Fig.7 Test conditions

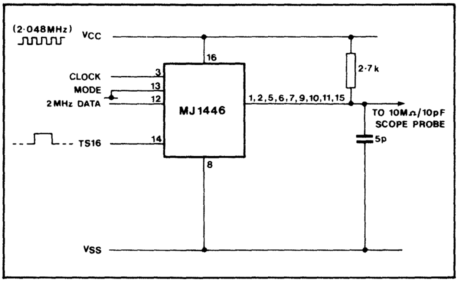


Fig.8 Test conditions

2 MBIT PCM SIGNALLING CIRCUIT

MJ1471

HDB3 OR AMI ENCODER/DECODER

The MJ1471 is an encoder/decoder for pseudo-ternary transmission codes. The codes are true Alternate Mark Inversion (AMI) or AMI modified according to HDB3 rules (CCITT Orange Book Vol 111-2, Annex to Rec.G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding and all ones detection (AIS). In addition a loop test function is provided for terminal testing.

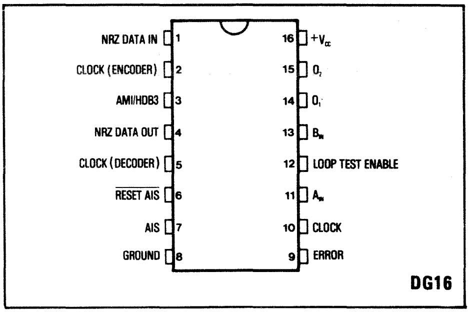


Fig.1 Pin connections

FUNCTIONS

- 5V ±5% Supply — 40mA Max.
- AMI or HDB3 Operation — TTL Selectable
- Loop Back Facility
- 'All Ones' Error Monitor to Detect Loss of Synchronising Word (Time Slot Zero)
- Error Monitor of HDB3 Incoming Code
- Decoded Data in NRZ Form

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data In
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. AMI/HDB3
MJ1471 operates in HDB3 if pin 3 is at logic '1'. AMI if pin 3 is at logic '0'.

4. NRZ Data out
Decoded data from ternary inputs A_{in}, B_{in}.

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}} = 1$ period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}} = 1$ periods.

Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been decoded i.e. 3 '1's of the same polarity.

10. Clock
OR function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', OR function of O_1, O_2 when pin 12 = '1'.

11, 13. A_{in}, B_{in}
Inputs representing the received ternary PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the clock decoder. A_{in} and B_{in} may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous.

When pin 12 = '1' O_1 is connected internally to A_{in} and O_2 to $B_{\overline{in}}$. Clock becomes the OR function of O_1 O_2. **N.B.** a decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in loop back.

14, 15, O_1, O_2
Outputs representing the ternary encoded PCM AMI/HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length.

16. $+V_{CC}$
Positive 5V ±5% supply.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ±0.25V
Ambient temperature T_{amb} = 0°C to +70°C

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,3,5,6 10,11,12,13	-0.3		0.8	volts	
Low level input current	I_{IL}				50	µA	V_{IL} = 0V
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	V_{IH} = 5V
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 0.80µA
		4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0v All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs.9, 14
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs.10, 14
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.8, 9, 14. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.9, 14
tpd1A-tpd1B				20	ns	Figs.9, 14
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = 1, Figs.9, 14
Setup time of NRZ data in to Clock (Encoder)	ts3	50			ns	Figs.7, 9, 14
Hold time of NRZ data in	th3	55			ns	Figs.7, 9, 14
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.12, 14
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.11, 14
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.13, 14
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.7, 10, 14. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.7, 10, 14
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.7, 10, 14
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	30			ns	Figs.7, 13, 14
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	100			ns	Figs.7, 13, 14
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.13, 14

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3)
2. The decoded NRZ output is delayed by 4 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4)

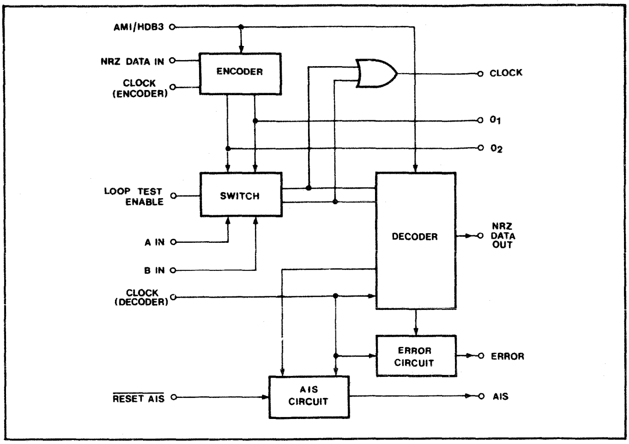


Fig. 2 MJ1471 Block diagram

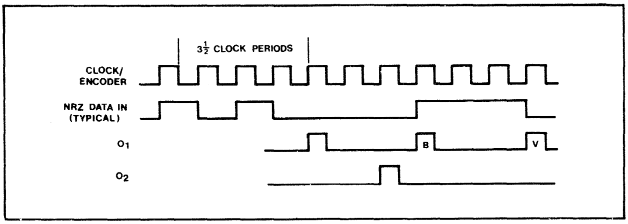


Fig. 3 Encode waveforms

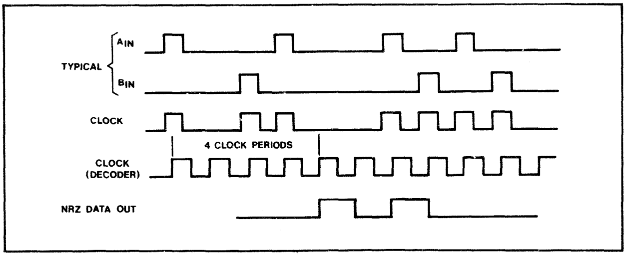


Fig. 4 Decode waveforms

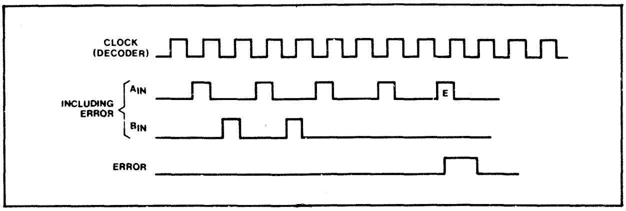
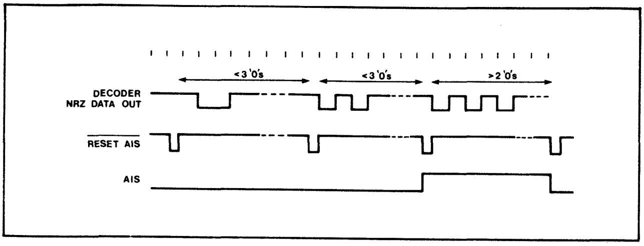


Fig. 5 HDB3 error output waveforms



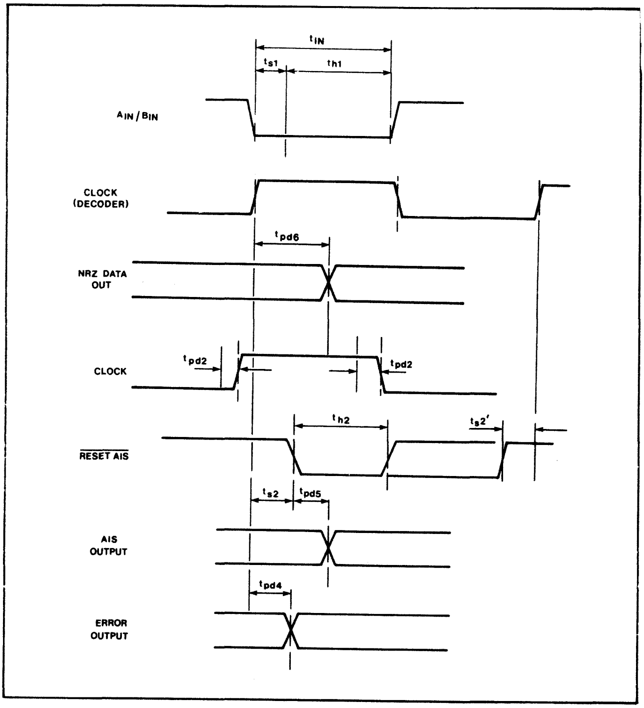


Fig. 7 Decoder timing relationship

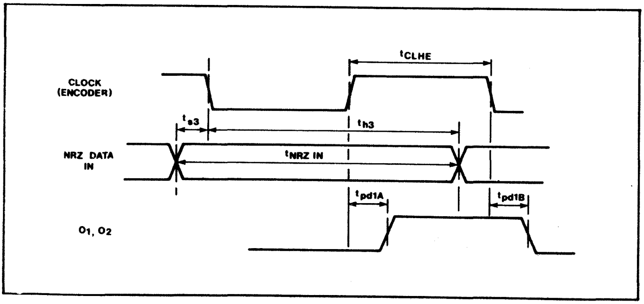


Fig. 8 Encoder timing relationship

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance:	Chip to Case	Chip to Amb.
	40°C/Watt	120°C/Watt

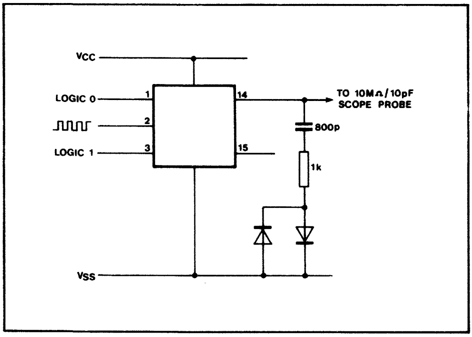


Fig. 9

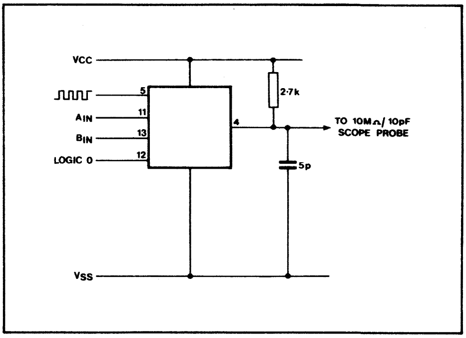


Fig. 10

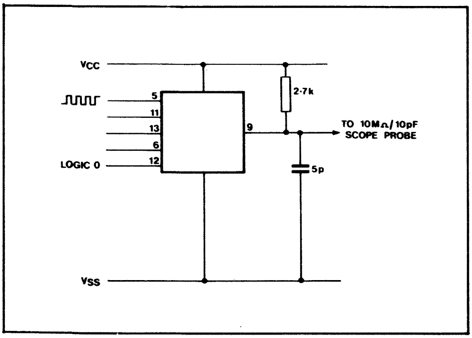


Fig. 11

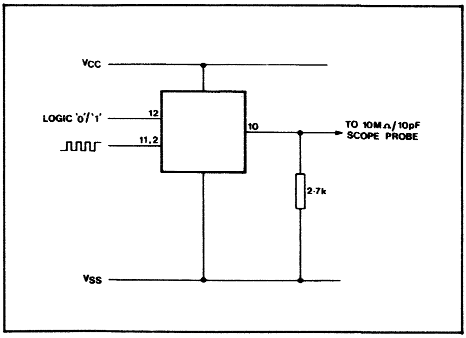


Fig. 12

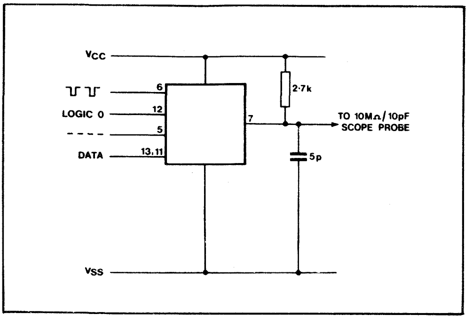


Fig. 13

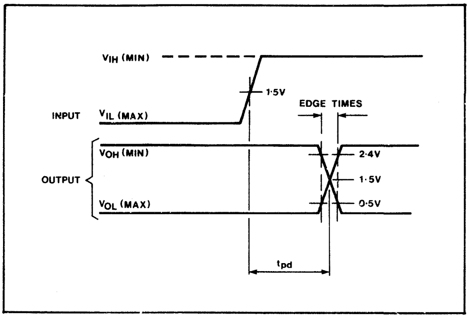


Fig. 14 Test timing definitions

PLESSEY Semiconductors

ADVANCE INFORMATION

PCM 'A'-LAW CODEC

MJ1480 DIGITAL CONTROLLER SL1480 ANALOGUE PROCESSOR

8-BIT COMPANDED 'A'-LAW A-D AND D-A CONVERTER

The bipolar SL1480 and NMOS MJ1480 integrated circuits together form a Codec system for the analogue to digital and digital to analogue conversion of telephony speech signals to PCM, as shown in Fig.2. The system is suitable for use in asynchronous transmission equipment and synchronous subscriberline cards. The conversion law is non-linear and conforms to the A law as defined by the CCITT Orange Book, Vol III—2, G711. The SL1480 performs the analogue signal processing functions, and the MJ1480 provides the successive approximation register and PCM interface circuits. The system is designed to operate at a 2.048MHz clock rate and requires a channel clock input to initiate an encode-decode cycle. Digital inputs and outputs are in serial NRZ form with alternate bits inverted, synchronous with the clock. An encode is performed in 11 clock periods and a decode is instantaneous. The system can serve 16 analogue channels at a sampling rate of 8kHz when provided with a 2.048MHz clock and the appropriate channel clocks. An internal two-channel multiplexer is provided to facilitate the use of external multiplexers on both the input and output analogue channels.

The analogue inputs are differential to provide good rejection against clocks and other common mode signals. The analogue outputs are high speed operational amplifiers which are driven by the D-A converter during decode; when the Codec is in encode mode or an output is not selected it is set to zero volts. The relationship of digital information on the PCM highways and analogue samples on the two channels is shown in the timing diagrams, Figs.3a and 3b.

The encode cycle consists of two guard bits, seven encode bits and two further guard bits. When a 2.048MHz clock is used the encode sample period is 4μs. The aperture error is sufficiently small with this length of sample that an input sample and hold is unnecessary and provides no performance advantage.

ABSOLUTE MAXIMUM RATINGS

Electrical

SL1480

V_{IN} to Gnd	+5.5V
V_{EE} to Gnd	-5.5V
Digital inputs (pins 1-10, 12)	+5.5V to -0.5V
Analogue inputs (pins 18-21)	V_{CC} to V_{EE}
Differential input voltage	±3.0V V18—V19 V20—V21

MJ1480

V_{DD} to Gnd	+7V
Logical inputs	-0.3V to +7.0V

Thermal

SL1480 and MJ1480

Chip-to-case thermal resistance	15°C/Watt
Chip-to-case ambient thermal resistance	60°C/Watt
Operating ambient temperature	0°C to +70°C
Storage temperature	-55°C to +175°C
Maximum junction temperature	+150°C

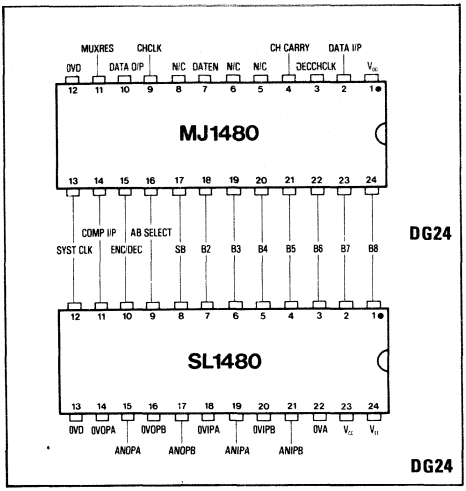


Fig.1 Pin connections SL1480 and MJ1480 (top view)

FEATURES

- Two Chip System May Be Shared Up To 16 Channels
- Includes Internal Two Channel Multiplexer
- Low Power Consumption — Equivalent to 76mW per Channel in Multiplexed Mode (8 Channels)
- Meets All Relevant CCITT Specifications
- May be Simply Designed Into a 32 Channel Security Zone Channel Bank
- Fast A-D Conversion Time, 6μs (With 2.048MHz Clock)
- Requires No External Components For Two Channel Application
- Highly Stable On-Chip Voltage Reference
- Supply Requirements ±5V, ±5%
- All Digital Inputs and Outputs TTL Compatible

APPLICATIONS

- 30/32 Channel PCM Systems
- Data Acquisition
- Telemetry
- Digital Signal Processing
- Speech Synthesis
- Voice Recognition

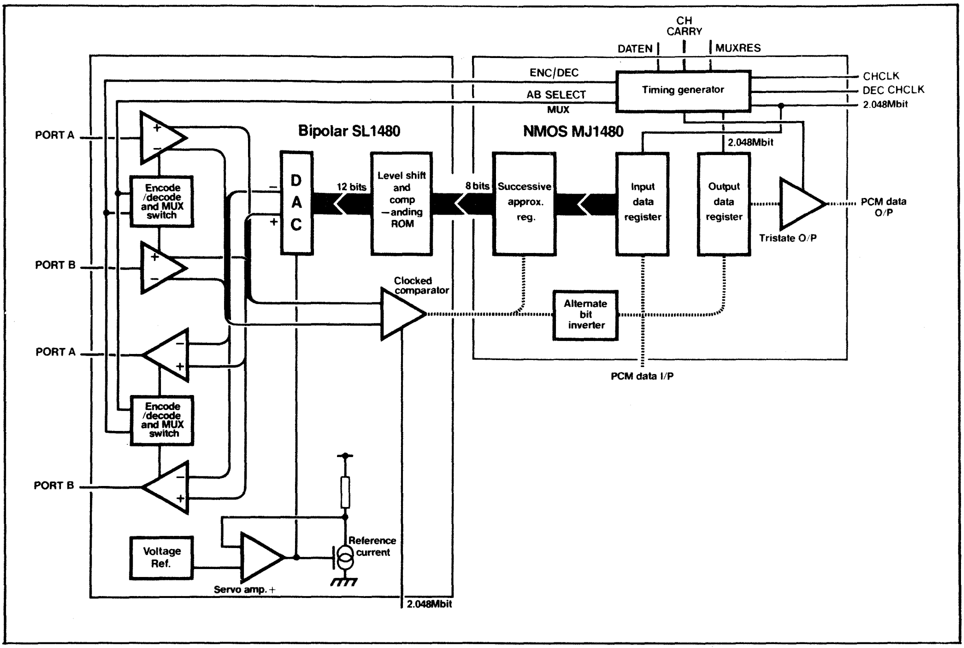


Fig.2 Codec block diagram and partitioning

FUNCTIONAL PIN DESCRIPTION

SL1480

Pin No.	Symbol	Description	
1	B8	Data, bit 8 (LSB)	D-A Converter inputs — 8 bits, 'A'-law companded.
2	B7	Data, bit 7	
3	B6	Data, bit 6	
4	B5	Data, bit 5	
5	B4	Data, bit 4	
6	B3	Data, bit 3	
7	B2	Data, bit 2	
8	SB	Data, sign bit (MSB)	
9	AB SELECT	Input and output multiplexer control. Normally connected to MJ1480 pin 16. A 'High' selects port B, 'Low' selects Port A.	
10	ENC/DEC	Select input or output amplifiers. 'Low' causes input to be selected. 'High' causes output to be selected.	
11	COMP O/P	Output of the successive approximation comparator, connects to pin 14, MJ1480. The comparator is a clocked master-slave circuit and compares the analogue input signal with the output of the D-A converter. The comparator samples the comparison on the positive clock transition and the result appears on pin 11 after the negative clock transistion. The comparator output is high if the analogue input is greater than the decoded digital input.	
12	SYST CLK	System clock. 2.048 MHz for 30/32 channel PCM channel bank.	
13	0VD	Digital earth	
14	0VOPA	Analogue earth	Port A
15	ANOPA	Analogue output	
16	0VOPB	Analogue earth	Port B
17	ANOPB	Analogue output	
18	0VIPA	Analogue earth	Port A
19	ANIPA	Analogue input	
20	0VIPB	Analogue earth	Port B
21	ANIPB	Analogue input	
22	0VA	Analogue earth	
23	V_{CC}	+5V ±5% supply	
24	V_{EE}	-5V ±5% supply	

MJ1480

Pin No.	Symbol	Description	
1	V_{DD}	+5V ±5% supply	
2	DATA I/P	Data input from PCM receive highway. Clocked by positive edge of clock.	
3	DECCH CLK	Decode only channel clock input. Positive going edge on this pin causes a decode output. This input must be low if the channel clock (pin 9) is used.	
4	CH CARRY	Channel carry will go high 8 system clock periods after the positive edge of a channel clock. This allows cascading of Codecs with no need for multiple channel clocks.	
5	N/C		
6	N/C		
7	DATEN	A '0' on this input will allow data out onto the PCM transmit highway. A '1' will cause the output to be off.	
8	N/C		
9	CHCLK	Channel clock input pin. A positive edge on pin 9 will start an encode cycle which lasts 11 system clocks. This is followed by a decode until the next channel clock. If the Decode channel clock (pin 3) is used pin 9 must be high.	
10	DATA O/P	Data output onto PCM transmit highway. The output is an open drain allowing wired-OR connection to other devices.	
11	MUXRES	A '1' resets AB SELECT output to 'High' (see Note 1 and timing diagram, Fig.3a), clocked on negative edge of system clock.	
12	OVD	Digital earth.	
13	SYST CLK	System clock, 2.048MHz for 30/32 channel PCM channel bank	
14	COMP I/P	Comparator input; connect to pin 11, SL1480.	
15	ENC/DEC	Encode/decode select output; connect to pin 10, SL1480.	
16	AB SELECT	Port A/Port B select output; connect to pin 9, SL1480.	
17	SB	Data, sign bit (MSB)	Data output of successive approximation register (to SL1480)
18	B2	Data, bit 2	
19	B3	Data, bit 3	
20	B4	Data, bit 4	
21	B5	Data, bit 5	
22	B6	Data, bit 6	
23	B7	Data, bit 7	
24	B8	Data, bit 8 (LSB)	

NOTES
1. MUXRES will reset AB SELECT output to a 'High' when either a channel clock or a decode only channel clock is received, see timing diagram (Fig.3a).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Ambient temperature T_{amb} = 0°C to +70°C
V_{CC} = +5V ± 5%, V_{EE} = −5V ± 5% (SL1480)
V_{DD} = +5V ± 5% (MJ1480)

SL1480

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static						
Positive supply current	I_{EE}		25	50	mA	Pins 1-10, 12, 19-21 = 0V
Negative supply current	I_{CC}		25	50	mA	" "
Logic '1' input voltage pins 1-10, 12	V_{IH}	2.0		V_{cc} + 0.5	V	
Logic '1' input current pins 1-10, 12	I_{IH}			0.2	mA	$V_{IH} = V_{cc}$
Logic '0' input voltage pins 1-10, 12	V_{IL}	0		0.8	V	
Logic '0' input current pins 1-10, 12	I_{IL}			−0.36	mA	V_{IL} = 0.4V
Logic '1' output voltage pin 11	V_{OH}	2.7			V	I_{OH} = 50μA
Logic '0' output voltage pin 11	V_{OL}			0.5	V	I_{OL} = − 1.0mA
Analogue Inputs						
Input impedance	R_{IN}	2.4		7.0	kΩ	Input code X0000000 *
Input bias current	I_B			0.15	mA	Encode mode, port A or port B selected.

ELECTRICAL CHARACTERISTICS, SL1480 (CONTINUED)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Encode offset voltage	V_{IN}	-32		+32	mV	
Input offset current ratio		0.9		1.1		
Temperature coefficient of ΔV_{IN}	$\frac{\Delta V_{IN}}{T}$				V/°C	
Temperature coeff. of input bias current	$\frac{I_B}{T}$				μA/°C	
'Crash level'		0.75		0.85	V	Comparator O/P = 1, code in = 11111111
		-0.75		-0.85	V	Comparator O/P = 0, code in = 01111111
Min. step size	$V_{step\,E}$		0.4		mV	
0dm0 level			0.40		Vrms	
Analogue Outputs (pins 14-17)						
Offset voltage (encode selected)	V_{offe}	-50		+50	mV	
Offset voltage (decode selected)	V_{offd}	-50		+50	mV	Code in = X0000000*
Minimum step size	$V_{step\,D}$		0.5		mV	
Output voltage (max. code in)	V_{OMAX}	±0.94		±1.03	V	Code in = X1111111*
Output noise	V_{ON}			-88	dBm	Code in = 10000000 Decode selected Bandwidth = 1 MHz
Temp. Coeff. decode gain	$\frac{V_{OMA}}{T}$	-200		+200	ppm/°C	
Output rise time	tr				ns	Code in changed from 01111111—11111111
Max. overshoot	V_{OV}				V	
Output current					mA	
Crosstalk						
Encode to Decode	V_{CED}			-75	dB	Code in 1000000 analogue in 0.5 Vrms at 850 Hz. Port A or B in to Port A or B out
Encode interchannel crosstalk	V_{CEE}			-73	dB	Port A = 0.50 Vrms 850 Hz. Port B = 0.05 Vrms 2.4 KHz Crosstalk measured A→B (or vice versa)
Decode interchannel crosstalk	V_{CDD}			-80	dB	Port A = 850 Hz, 0dBm0 measure Port B, or vice versa.
Decode/Encode crosstalk	V_{CDE}			-73	dB	Port A or B output = 850 Hz 0dBm0 Port A or B input 850 Hz, 0.05 Vrms

*X specifies a 'don't care' condition

MJ1480

Static						
Supply current	I_{DD}			80	mA	
High state output voltage, pin 4, 15-24	V_{OHB}	2.7			V	$I_O = 50\mu A$
Low state output voltage, pin 4, 15-24	V_{OLB}			0.5	V	$I_O = -1\,mA$
Low state output voltage, pin 10	V_{OLA}			0.5	V	$I_O = -2\,mA$
Offstate leakage current, pin 10	I_{OO}			5	μA	$V_{OUT} = 2.7V$
High state input voltage, all inputs	V_{IH}	2.4			V	
Low state input voltage, all inputs	V_{IL}			0.8	V	
High state input current	I_{IH}			20	μA	$V_I = 2.7V$
Low state input current	I_{IL}			20	μA	$V_I = 0.4V$
Dynamic						
Propagation delay, clock to B1-B7, SB	tp_{SAR}			150	ns	
Propagation delay, clock to ENC/DEC	tp_{ED}			150	ns	
Propagation delay, clock to AB SELECT	tp_{AB}			150	ns	
Delay, system clock to Data I/P	t_{DIP}	-11			ns	
Propagation delay, channel clock to Bit 1 Data O/P	tp_{CCD}	20		130	ns	
Propagation delay, system clock to Bit 2-8, Data O/P	tp_{CD}	20		270		
Propagation delay, system clock to channel carry	tpccc	20		120	ns	
Set up time, system clock to MUX RES	t_{STSO}	50			ns	
Hold time, MUX RES	t_{HTSO}	100			ns	
Set up time, CH CLK to system clock	t_{SCC}	200			ns	
Delay time, system clock to CH CLK	t_{DCC}	100			ns	

SL1480 and MJ1480 Combined Performance (see Fig.2)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Quantising distortion	Q_{DN}					
Analogue-Digital		-15.3			dB	V_{IN} = -55dBm0 See Note 1 and Fig.4
		-30.3			dB	V_{IN} = -40dBm0
		-34.4			dB	V_{IN} = -34dBm0
		-35.6			dB	V_{IN} = -27dBm0
		-35.6			dB	V_{IN} = -6dBm0
Digital-Analogue		-15.3			dB	V_{OUT} = -55dBm0 See Note 2 and Fig.7
		-30.3			dB	V_{OUT} = -40dBm0
		-34.4			dB	V_{OUT} = -34dBm0
		-35.6			dB	V_{OUT} = -27dBm0
		-35.6			dB	V_{OUT} = -6dBm0
Linearity						
A-D noise signal	G_{NAD}			0.25		V_{IN} = -55dBm0, see Fig.5 and note 1
				0.50		V_{IN} = -60dBm0, see Fig.5 ··
A-D, 820Hz sine signal	G_{SAD}			0.25		V_{IN} = +3dBm0, see Fig.6
D-A noise signal	G_{NDA}			0.25		V_{IN} = -55dBm0, see Fig.8 and note 2
				0.50		V_{IN} = -60dBm0, see Fig.8 ··
D-A sine signal	G_{SDA}			0.25		V_{IN} = +3dBm0, see Fig.9

NOTES
1. V_{IN} is band-limited Pseudo-Random Noise in accordance with CCITT recommendation 0.131
2. Input signal is a digital equivalent of V_{IN} (Note 1)

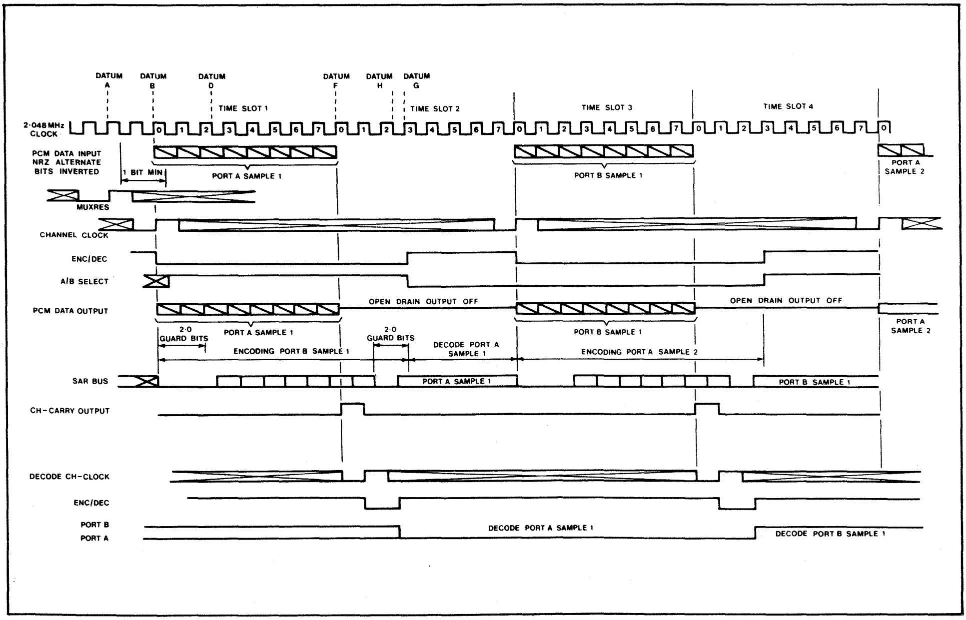


Fig.3a Codec interfacing waveforms

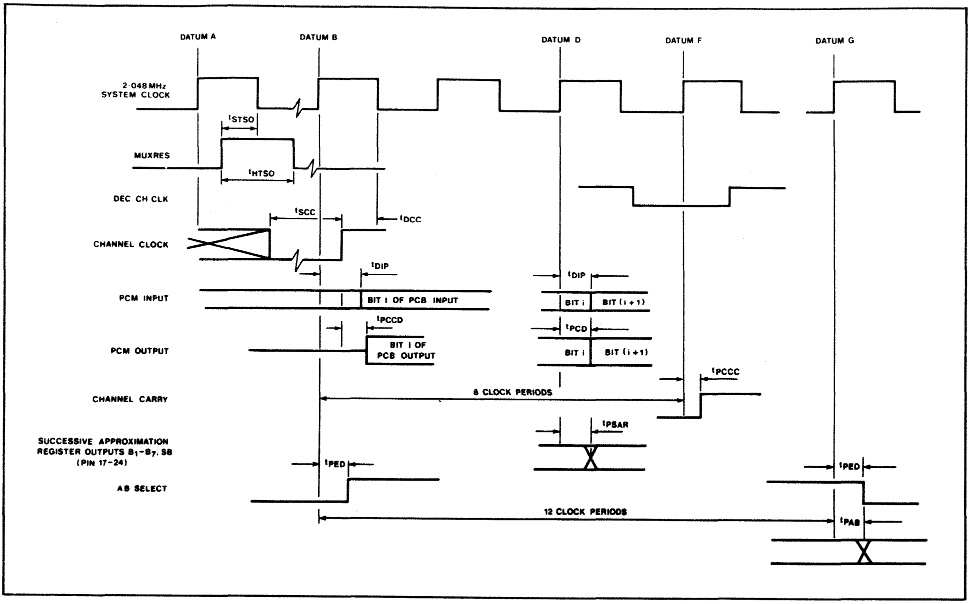


Fig.3b Codec detailed timing (all times in nanoseconds)

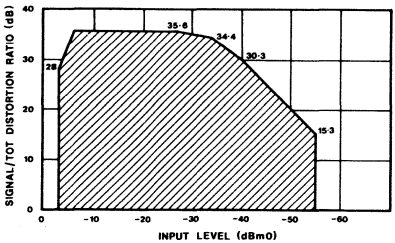


Fig.4 Quantizing distortion (encoder) as a function of input level (CCITT G712, Method 1)

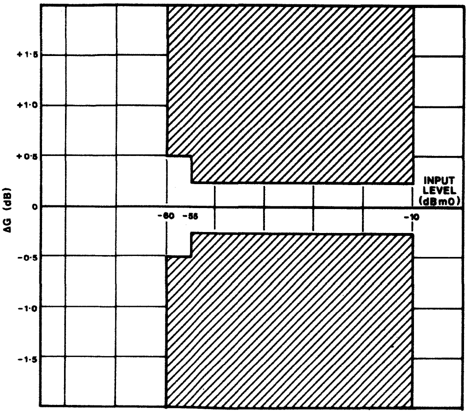


Fig.5 Variation of gain with input level (encoder) (CCITT G712, Method 1a)

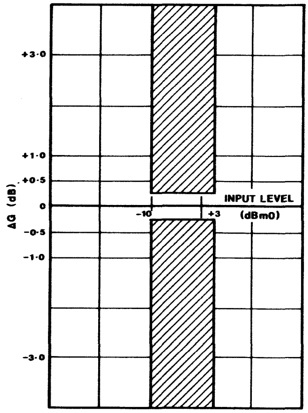


Fig.6 Variation of gain with input level (encoder) (CCITT G712, Method 1b)

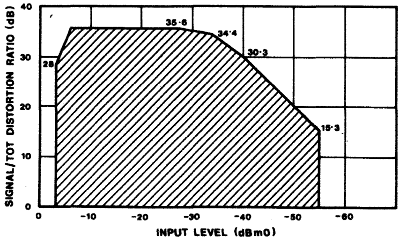


Fig.7 Quantizing distortion (decoder) as a function of output level (CCITT G712, Method 1)

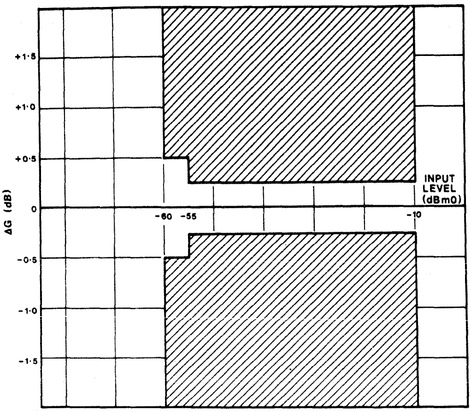


Fig.8 Variation of gain with input level (decoder) (CCITT G712, Method 1a)

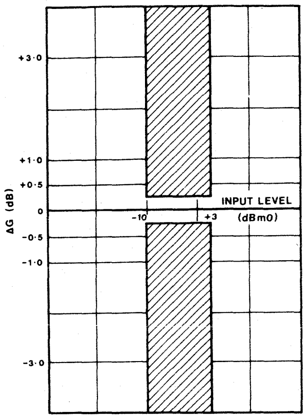


Fig.9 Variation of gain with input level (decoder) (CCITT G712, Method 1b)

APPLICATION NOTES

Input Amplifier

The input amplifier is a differential amplifier with both inputs available. Each part has a separate amplifier and input multiplexing is performed by routeing the tail current to the selected input amplifier. The circuit is shown in Fig.10.

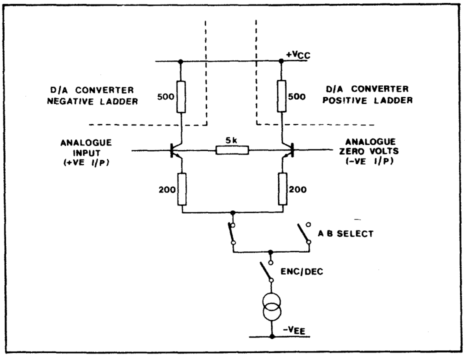


Fig.10 Input amplifier of SL1480

It is important to note that the input to the Codec is extremely broadband (Typ. 100MHz) and consequently care has to be taken to limit the noise bandwidth of the signal path leading up to the input. In addition, the impedance seen by each base of the input differential pair should be matched to reduce common mode signals (i.e. clocks etc.). Suitable configurations are shown in Figs.11a and 11b. The configuration shown in Fig.11a is only suitable for systems where each Codec input serves a single analogue channel. For applications where the signal input is derived from a multiplexer, the configuration shown in Fig.11b is more suitable as the bandwidth can be tailored for the required application.

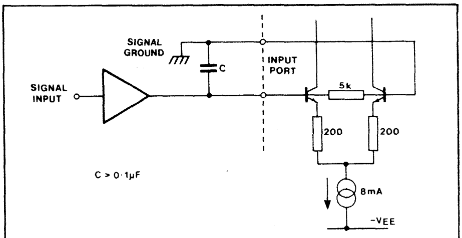


Fig.11a Input configuration for non-multiplexed applications

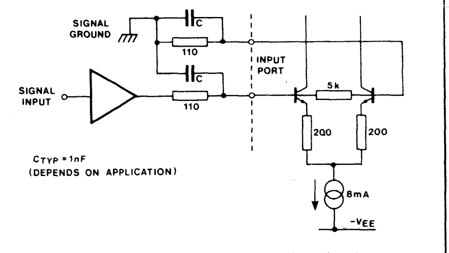


Fig.11b Input configuration for multiplexed applications

Voltage Reference

Input and output channel gains are referenced to an internal band gap reference voltage and can be expected to be extremely stable with time and temperature. A typical regulation characteristic is shown in Fig.12.

Output Amplifier

Each output port is the output of a high performance operational amplifier selected during decode periods and driven by the D-A converter. During encode or when the particular port is not selected the output is set to zero volts. A separate output signal earth is available for each amplifier to reduce crosstalk between channels.

Digital to Analogue Conversion

The Codec uses a successive approximation technique for encoding. The same D-A converter is used for encoding and decoding. The D-A converter is a composite structure. The 'A' law segments are selected by an R/2R resistor ladder and interpolation within each segment is performed by a group of binary weighted current sources (see Fig.13). The resistor current product formed by the converter is referenced directly to the device voltage reference ensuring excellent gain stability.

Digital Interface

The PCM interfaces to the codes are at the clock rate (2.048MHz) and are in NRZ form with alternate bits inverted. The Codec is designed to interface with a standard 2.048M bit PCM frame and the 8 bit words associated with a particular time slot are loaded and unloaded on receipt of a channel clock. If the Codec is being used in the 'decode only' mode then the time slot immediately preceding the decode channel clock is loaded. The relationship between analogue samples and digital PCM samples is shown in Fig.3a. Encoded analogue samples are output to the PCM highway by the next channel clock and decoded analogue samples are output to the appropriate analogue port immediately following the encode cycle. The selection of ports is controlled by the MJ1480 and alternate channel clocks select port A or port B. Synchronisation of the internal multiplexer to the PCM frame is accomplished by the MUXRES input.

The PCM output is an open drain device and up to four Codecs can be connected to a PCM highway and still allow a load equivalent to two low power Schottky loads to be driven. The output of a Codec is only active when data is being output; at all other times the output is open circuit. There is a data enable (DATEN) input to the Codec which allows a particular Codec to be disabled on a static or dynamic basis thus allowing concentration on a line-by-line basis to be performed in Subscriber Line Interface Circuit (SLIC)

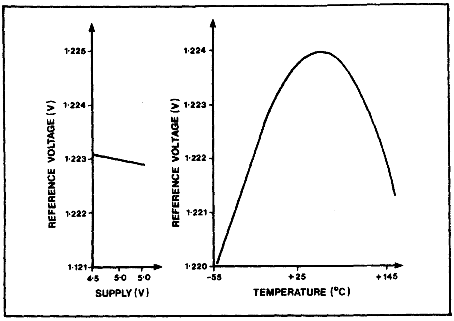
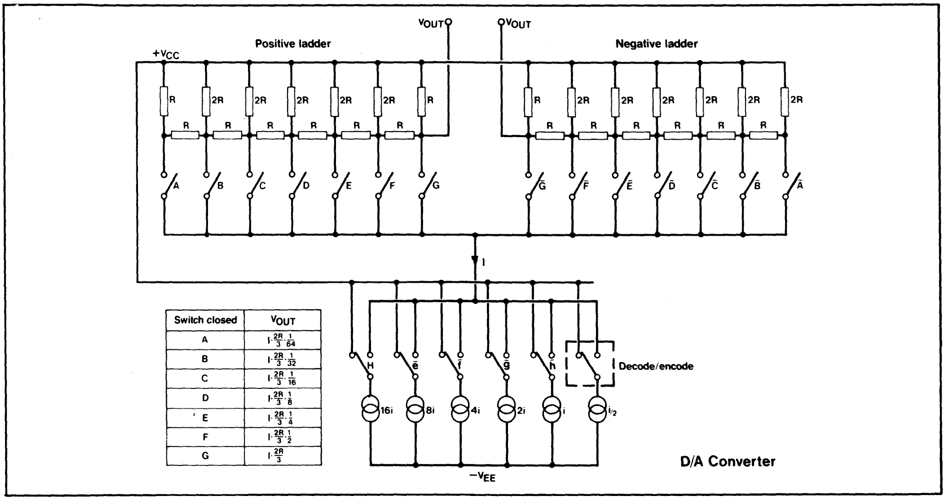


Fig.12 Regulation characteristics of the SL1480 voltage reference



Switch closed	V_{OUT}
A	$I \cdot \frac{2R}{3} \cdot \frac{1}{64}$
B	$I \cdot \frac{2R}{3} \cdot \frac{1}{32}$
C	$I \cdot \frac{2R}{3} \cdot \frac{1}{16}$
D	$I \cdot \frac{2R}{3} \cdot \frac{1}{8}$
E	$I \cdot \frac{2R}{3} \cdot \frac{1}{4}$
F	$I \cdot \frac{2R}{3} \cdot \frac{1}{2}$
G	$I \cdot \frac{2R}{3}$

Fig.13 D-A converter for the SL1480

An Eight Line Subscriber Interface

The circuit shown in Fig.14 is an eight analogue line system using the SL1480 + MJ1480 as an 'A' law Codec.

Filtering

Three technologies are recognised for antialias filtering the analogue input signal. This circuit uses active filters although LC or switched capacitor filters could be used (with appropriate gain adjustments). A significant problem with active filters is their relatively high broadband noise level. Consequently, to improve dynamic range the signal level at the filter output has been set at approximately +15dBm0 (relative to the Codec input). Noise in the output filter is not such a severe problem as broadband noise is not a significant performance hazard.

The particular filters used are a combination of thin film substrates and gain blocks provided by Plessey TAB1042 quad programmable operational amplifiers.

A similar system using 2912 type switched capacitor PCM filter has been developed. Full information is available from Plessey Semiconductors.

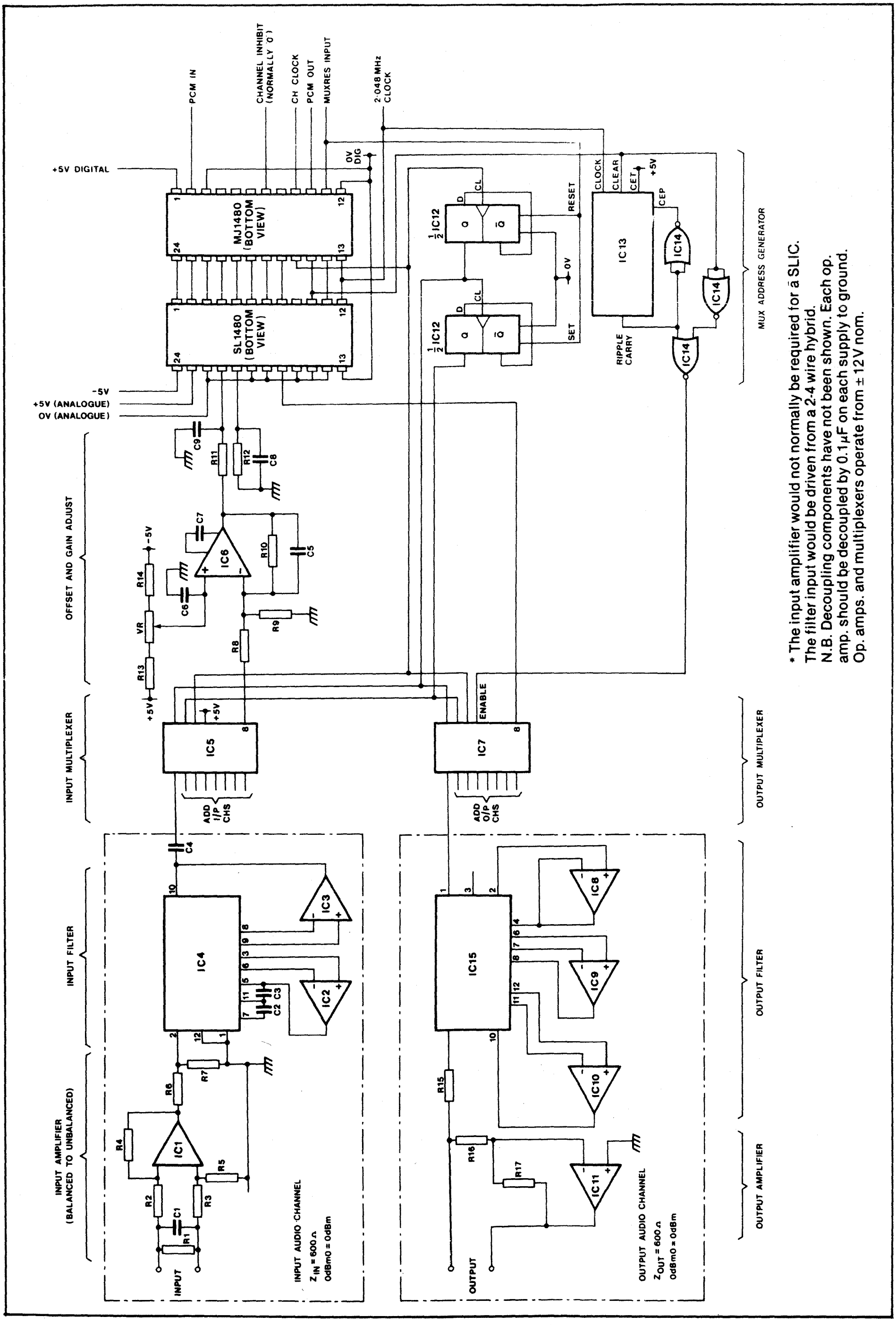
Multiplexing

Industry standard 1 to 8 multiplexers are used in this application. The internal multiplexer of the Codec is not used as to do so would necessitate a more complex multiplexing scheme with four 1 to 4 multiplexers being required. The selected multiplexers have adequate switching speed to cope with the system. A further advantage of this configuration is that it could be expanded to 16 channels by duplicating the analogue path and using the other Codec port. The address waveforms required by the multiplexers are shown in Fig.15.

Offset and Gain Adjust

The variable ON resistance of the multiplexer, coupled with the 5kΩ input impedance of the Codec mean that a buffer is required to prevent gain variations outside the required specification. This buffer also allows input offset adjustment by means of a preset resistor (or an autozero circuit if preferred). The buffer is preceded by an attentuator to reduce the relatively high signal level in the filter to that suitable for the Codec.

The bandwidth of this section should be limited to the minimum possible consistent with response times required by the multiplexed input. Bandwidth is controlled by R11, C9 and in practice full advantage cannot be taken of this bandwidth as linearity at low levels deteriorates slightly for larger values of C8 and C9. A compromise between linearity and signal-to-noise ratio can be reached as the performance curves of Figs.16a and 16b show:



* The input amplifier would not normally be required for a SLIC.
The filter input would be driven from a 2-4 wire hybrid.
N.B. Decoupling components have not been shown. Each op. amp. should be decoupled by 0.1μF on each supply to ground.
Op. amps. and multiplexers operate from ± 12V nom.

Fig.14 An 8-channel synchronous multiplexed Codec

PARTS LIST FOR FIG. 14

INTEGRATED CIRCUITS

REF. NO.	FUNCTION	PART NO.	MANUFACTURER
IC1* IC2* IC3* IC8*	Op. Amp.	TAB 1042	Plessey
IC9* IC10* IC11*	Op. Amp.	TAB 1042	Plessey
IC5 IC7	Mux	MUX08, IH6108	PMI Intersil
IC6	Op. Amp.	NE5534	Mullard
IC12	CMOS dual D-type FF	4013	Any
IC13	CMOS 4 bit counter	40163	Any
IC14	CMOS Quad Nor gate	4001	Any
IC4	Transmit filter	S42026-A16-A3	Siemens
IC15	Receive filter	S42026-A15-A1	Siemens

RESISTORS

R1*	620Ω	R10	2.0kΩ
R2*	30kΩ	R11	110kΩ
R3*	30kΩ	R12	110kΩ
R4*	54kΩ	R13	2.0kΩ
R5*	54kΩ	R14	1.8kΩ
R6*	2.4kΩ	R15*	41Ω
R7*	2.2kΩ	R16*	17kΩ
R8*	9.1kΩ	R17*	33kΩ
R9	2.2kΩ	VR1	500Ω

CAPACITORS

C1*	0.01μF ± 20%
C2*	0.1μF ± 3%
C3*	0.1μF ± 3%
C4*	0.68μF ± 10%
C5	10pF ± 20%
C6	1μF ± 10%
C7	22pF ± 20%
C8	1nF ± 10%
C9	1nF ± 10%

* These components are required for each analogue channel.
TAB1042s used for IC1, 2, 3 should be biased with 7.5μA.
TAB1042s used for IC8, 9, 10, 11 should be biased with 75μA.

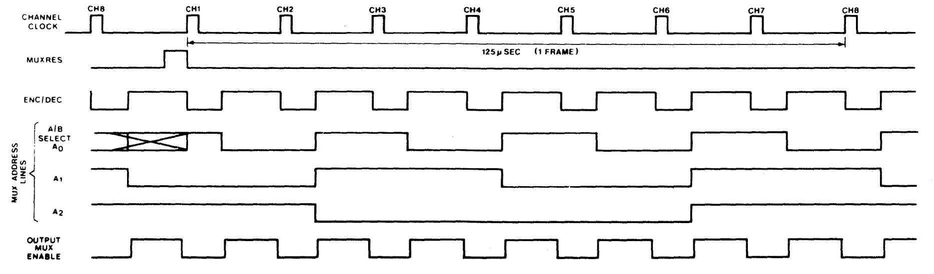


Fig.15a Multiplexer waveforms for an 8-channel multiplexed board

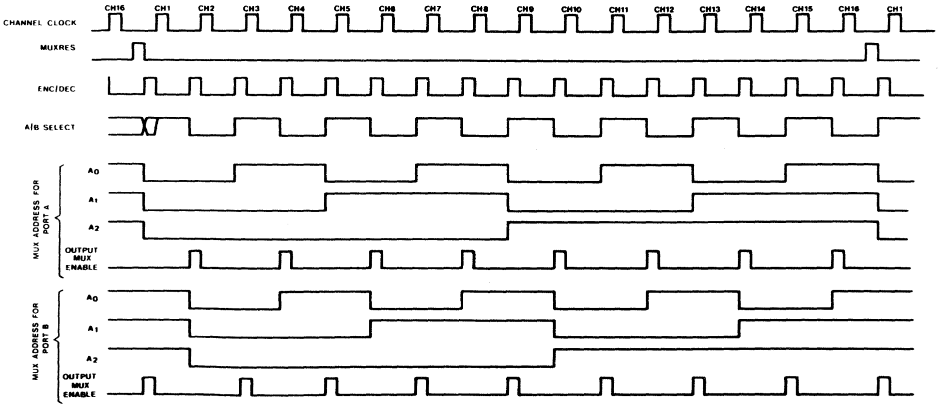


Fig.15b Multiplexer waveforms for a 16-channel multiplexed board

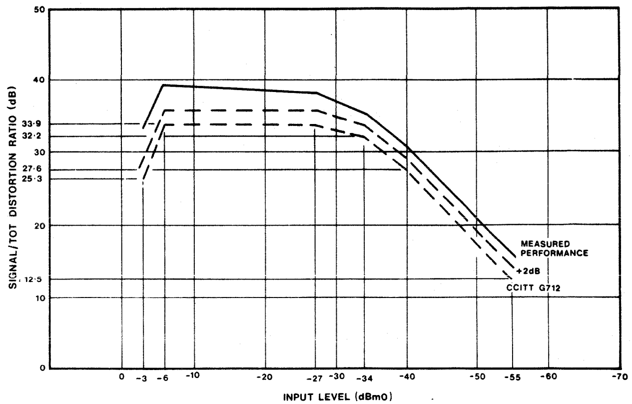


Fig.16a Encode Q_D measurements, multiplexed board (noise source)

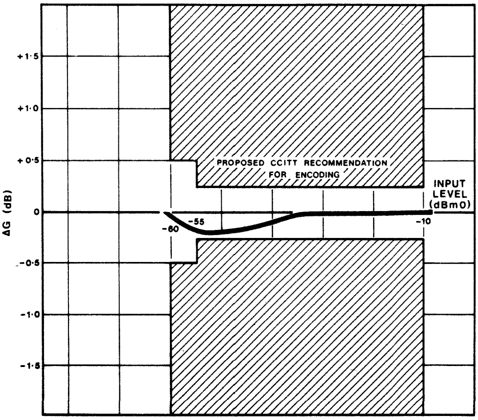


Fig.16b Encode linearity of multiplexed board (noise source)

Bandwidth Calculation

From Fig.15, the multiplexer address waveforms, we can see that the total period available to switch channels through the input multiplexer to the Codec input is 2.5 time slots (20 clock periods or 9.76μs). There is a delay to turn on the multiplexer, consisting of an address generation time, t_{add}, and a multiplexer turn on time, t_{onmux}, which must be subtracted from the 2.5 time slots before the bandwidth of input buffer can be calculated.

$t_{add} = t_{pA/B}$ (clock to AB sel)
$+ 2xt_{pa}$ (clock to Q for IC 12)
$= (150 + 2 \times 250)$ ns
$t_{onmux} = 2.1\mu s$ (PMI MUX08B)

The first bit to be set during the A/D conversion process is the sign bit and the worst case deviation for this decision is from full scale to zero. For accurate sign bit determination the input must be accurate to within ½ LSB. It is assumed that the single time constant ($R_{11}C_9 = \gamma$) controls the response time.

Full scale for an 'A' law codec = 2048 LSB steps.
now $V = V_{IN}(1 - e^{-t/\gamma})$ ...(1)
V = output voltage
V_{IN} = input voltage
γ = time constant (i.e. $R_{11} \times C_9$)
t = response time
$V = (2048 - \frac{1}{2})$ units
V_{IN} = 2048 units
$t = (9.76 - 0.65 - 2.1)\mu s$ (see above)

equation (1) gives γ = 843 ns and using $R_{11} = 110\Omega$ gives a value for C_9 of 7.67 nF. However, the use of C_9 with a capacitance of this magnitude causes linearity problems and a satisfactory compromising value for C_9 is 1 nf.

Output Multiplexing

The output analogue signal path is considerably simpler than the input signal path and consists of the multiplexer and the output filter. Addressing for the output multiplexer

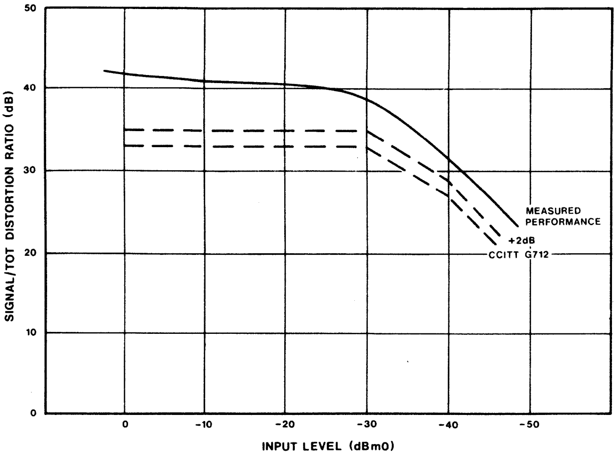


Fig.17a Decode Q_D measurements, multiplexed board (sine wave input)

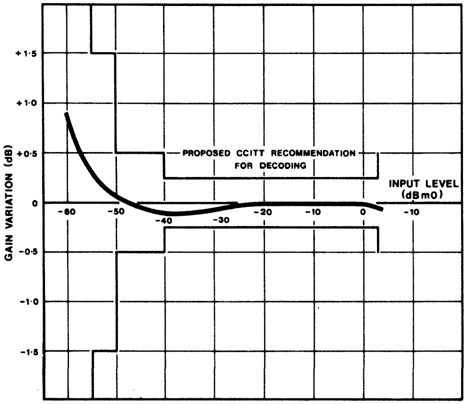


Fig.17b Decode linearity of multiplexed board (sine wave input)

is identical with that of the input multiplexer. However, it is important that the filter only samples the Codec PAM output when it is at its decoded analogue level. To achieve this an additional enable pulse is derived by IC13 and 14. The precise length of this pulse is not important but variations in its period will cause gain variations and channel clock jitter will cause additional noise on the recovered analogue signal.

The performance of the output channel is shown in Figs.17a and 17b.

Extension to 16 channels

This system could be extended to 16 channels merely by using both ports of the CODEC and duplicating the analogue signal paths. Multiplex addressing would be slightly more complex and the required waveforms are also shown in Fig.16.

An Asynchronous 30 channel PCM terminal for Transmission Equipment

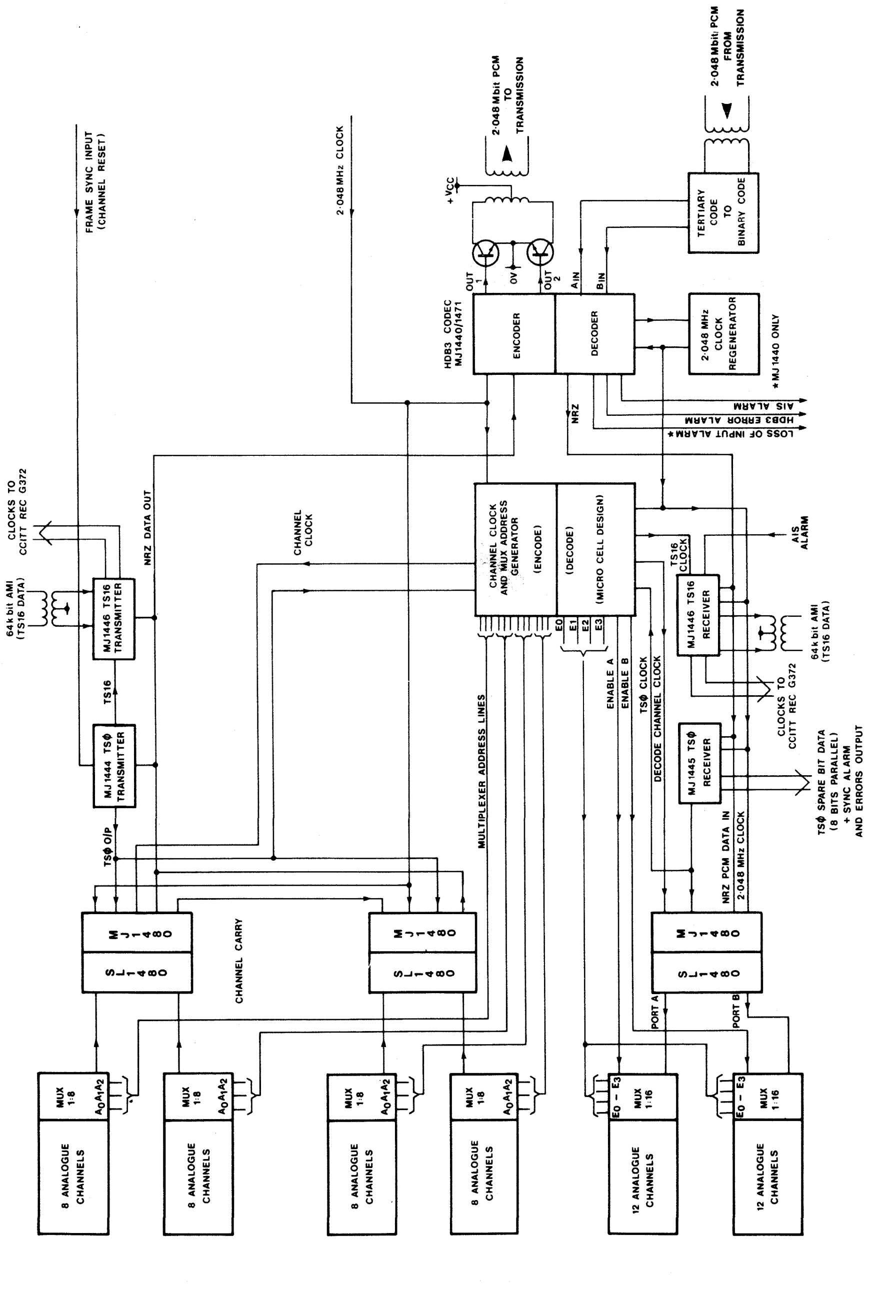
PCM transmission equipment differs from SLIC applications in that the digital send and receive highways are asynchronous. A block diagram of a suitable system is shown in Fig.18. The encode part of the system consists of two Codecs configured to serve 16 channels each, as in the SLIC example. In fact only 15 analogue channels are required as time slots zero and 16 are used for signalling.

Since the incoming and outgoing PCM streams are asynchronous a separate Codec is required for digital to analogue conversion. In this case the channel clock input (CHCLK) to the Codec is held high and the decode channel clock (DECCHCLK) is driven. This allows the Codec to decode the full 32 time slots (although only 30 would be used).

Synchronisation and data access to time slot zero and sixteen data bits can be provided by the MJ1444, MJ1445 and MJ1446 and conversion of the resulting 2.048M bit data stream to HDB3 or AMI ternary codes can be accomplished by the MJ1440 or MJ1471.

Conclusion

The Codec (SL1480 + MJ1480) is a flexible system which can be incorporated into both PCM transmission equipment and digital exchange subscriber interface circuits. In both applications it can provide considerable economies in both device count and cost while satisfying all the relevant CCITT performance specifications.



Asynchronous 2.048M bit PCM terminal for 32 analogue channels

Fig.18 Asynchronous 2.048M bit PCM terminal for 32 analogue channels

PLESSEY
Semiconductors

MJ2812, MJ2812M 32 WORDS x 8 BIT FIFO MEMORY
MJ2813, MJ2813M 32 WORDS x 9 BIT FIFO MEMORY

The MJ2812 and MJ2813 are 32-word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_0 - D_7$) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_0 - Q_7$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

Both the MJ2812 and MJ2813 have master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

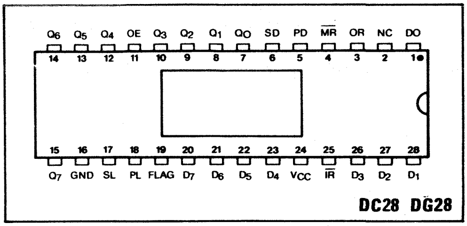


Fig. 1 MJ2812 (32 x 8) pin connections

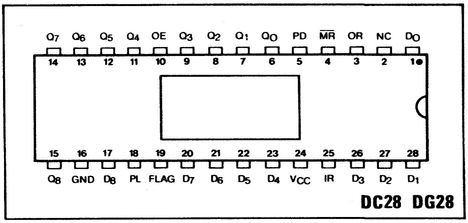


Fig. 2 MJ2813 (32 x 9) pin connections

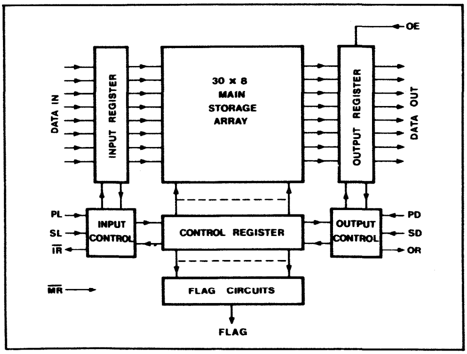


Fig. 3 MJ2812 simplified block diagram

FEATURES

- Serial or Parallel Inputs and Outputs (MJ2812 only)
- 32 Words x 8 Bits (MJ2812) and 32 Words x 9 Bits (MJ2813)
- Easily Stacked – Sideways or Lengthways
- Independent Reading and Writing
- Half-Full FLAG
- Data Rates up to 2.0 Mhz
- TTL – Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

OPERATING RANGE

Type number	Ambient temperature	V_{CC}	Ground
MJ2812/MJ2813	0°C to +70°C	5.0V ±5%	0V
MJ2812M/MJ2813M	−55°C to +125°C	5.0V ±5%	0V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Operating Range table (above)

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -0.3mA$
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 1.6mA$
Input high voltage	V_{IH}	2.5			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}			10	µA	$V_{IN} = 0V$
Input high current	V_{IH}			10	µA	$V_{IN} = 5.25V$
V_{CC} current	I_{CC}		70	114	mA	T_A = 0°C to +70°C
			70	120	mA	T_A = −55°C to +125°C

Switching Characteristics

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Maximum parallel load or dump frequency	f_p	2812/3	2.0			Mhz	
		2812M/3M	1.5			MHz	
Delay, PL or SL high to IR inactive	t_{IR+}	2812/3	25	90	200	ns	
		2812M/3M	20	90	250	ns	
Delay, PL or SL low to IR active	t_{IR-}	2812/3	60	140	350	ns	
		2812M/3M	55	140	400	ns	
Minimum PL or PD high time	$t_{pwH(P)}$	All			80	ns	
Minimum PL or PD low time	$t_{pwL(P)}$	All			100	ns	
Minimum SL or SD high time	$t_{pwH(S)}$	All			80	ns	
Minimum SL or SD low time	$t_{pwl(S)}$	All			80	ns	
Data hold time	$t_{h(D)}$	All		130	200	ns	
Data set-up time	$t_{s(D)}$	All			0	ns	to PL
		All			0	ns	to SL
Delay, PD or SD high to OR low	t_{OR+}	2812/3	45	110	240	ns	OE high
		2812M/3M	40	110	260	ns	OE high
Delay, PD or SD low to OR high	t_{OR-}	2812/3	64	180	400	ns	DE high
		2812M/3M	60	180	400	ns	DE high
Ripple through time	t_{PT}	2812/3	0.4	1.0	2.5	µs	FIFO empty
		2812M/3M	0.4	1.0	3.0	µs	FIFO empty
Delay, OR low to data out changing	t_{DH}	All	35	90		ns	PD=low
Delay, data out to OR high	t_{DA}	All	0	70		ns	PD=high
Minimum reset pulse width	t_{MRW}	2812/3			290	ns	
		2812M/3M			300	ns	
Delay, OE low to output off	t_{DO}	All			250	ns	
Delay, OE high to output active	t_{EO}	All			250	ns	
Delay from PL or SL low to FLAG high or PD or SD low to FLAG low	t_{DF}	All			1.0	µs	
Input capacitance	C_I	All			7	pF	

NOTES
1. IR is active high on MJ2813 and active low on MJ2812
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

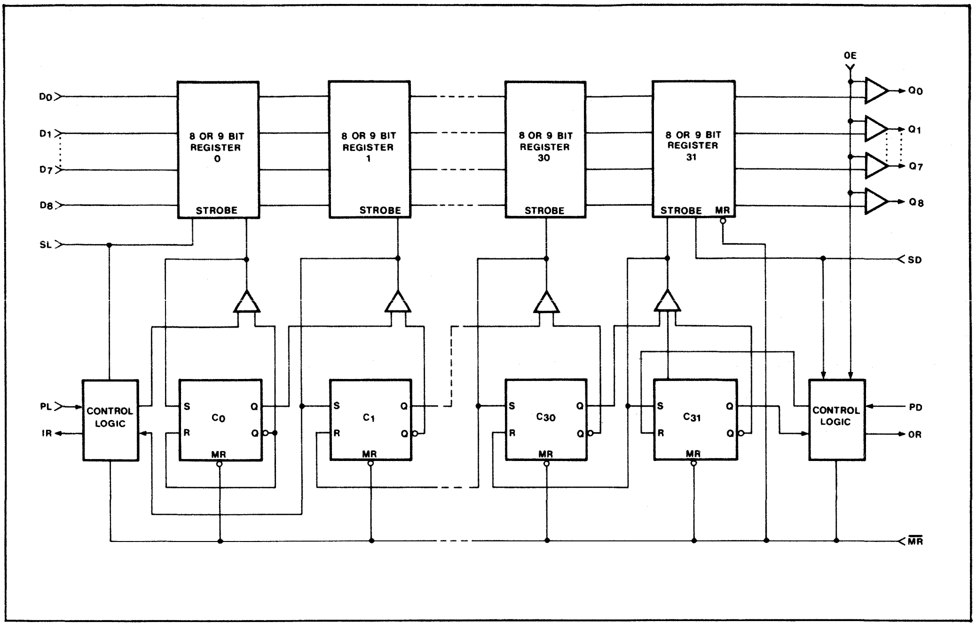


Fig. 4 Logic block diagram

MJ2812 AND MJ2813 FIFO OPERATION

The MJ2812 and MJ2813 FIFO's consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the (n)th data register, simultaneously setting the (n+1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused IR to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the IR output signals).

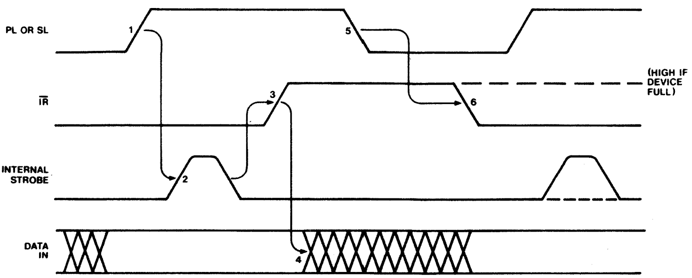
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register than 'bubbles' back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

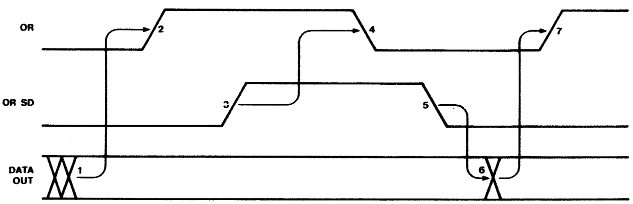
ABSOLUTE MAXIMUM RATINGS

Storage temperature	−65°C to +150°C
Temperature (ambient) under bias	−55°C to +125°C
Voltage on any pin w.r.t. ground (0V)	−0.3V to +9V
DC input voltage	−0.3V to +6V



MJ2812 INPUT TIMING

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.



MJ2812 OUTPUT TIMING

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The MJ2813 pattern is similar, but IR is active high instead of active low.

Fig. 5 MJ2812 timing diagram

Because the input ready signal is active low on the MJ2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812s connected end-to-end store 31n+1 words (instead of 32n). The MJ2813 stores 32n words in this configuration, because IR is active high and does dump the last word written into the second device.

Flag Output

A flag output is available on the MJ2812 and MJ2813 to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1µs of the 14th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1µs of the 20th PD or 160th SD high-low transition, ie. when 13 words remain in the memory.

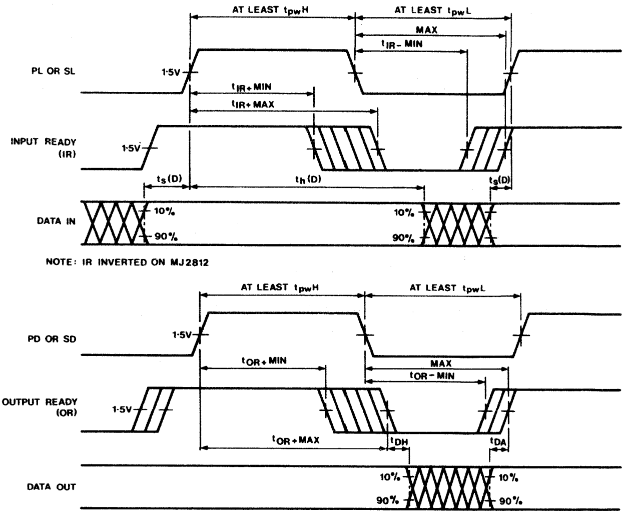
Serial Input and Output (MJ2812 Only)

The MJ2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_O input.

The SL signal operates just like the PL input, causing IR to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the Q_7 output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig. 6 Timing diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.

2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

3. If PD is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least t_{OR+}) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.

4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.

5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.

6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.

7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

PLESSEY
Semiconductors

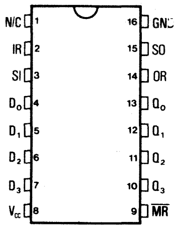
MJ2841

64-WORD x 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word D_0-D_3 under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs Q_0-Q_3. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows if FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.



DG16
DP16

Fig.1 Pin connections (top view)

FEATURES

- Single 5V Supply
- 1.75MHz Guaranteed Data Rate (Typically 4MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +125°C
Ambient operating temperature	-10°C to +85°C
Lead temperature (soldering, 10s max.)	330°C
Voltage on any pin with respect to ground	-0.3V to +7V

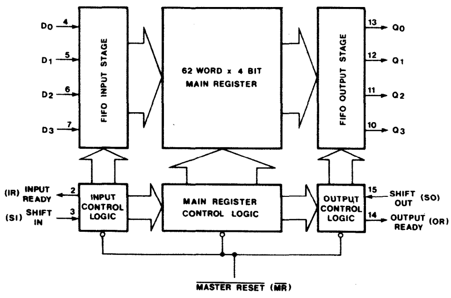


Fig.2 Block diagram

MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs D_0-D_3 by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs Q_0-Q_3. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

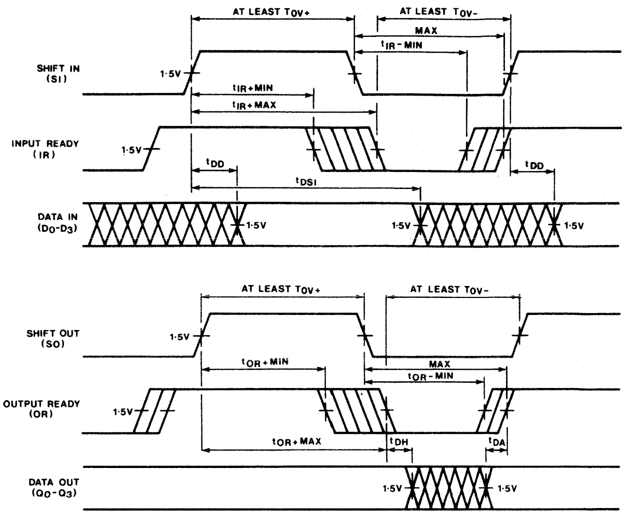
Supply voltage (V_{CC}) = +5V ±5%, T_{amb} = 0°C to +70°C
Typical Values at V_{CC} = 5V and T_{amb} = +25°C
All voltages with respect to ground

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O/P high voltage	V_{OH}	2.7	3.2		V	I_{OH} = -0.2mA
O/P low voltage	V_{OL}		0.2	0.5	V	I_{OL} = 2mA
I/P high level	V_{IH}	2.5			V	
I/P low level	V_{IL}			0.8	V	
I/P leakage current	I_{IL}	-5		+10	μA	V_{IN} = 0V or 5V
Supply current	I_{CC}		50	81	mA	

Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. SI or SO frequency	f_{MAX}	1.75	4.4		MHz	
Delay, SI high to IR low	$t_{IR}+$		50	120	ns	
Delay, SI low to IR high	$t_{IR}-$		80	200	ns	
Min. time SI and IR both high	$t_{OV}+$		<25	45	ns	
Min. time SI and IR both low	$t_{OV}-$		<25	45	ns	
Data release time	t_{DSI}		45	110	ns	
Data set-up time	t_{DD}		45	110	ns	
Delay, SO high to OR low	$t_{OR}+$		80	190	ns	
Delay, SO low to OR high	$t_{OR}-$		120	290	ns	
Ripple through time	t_{PT}		2.5	7	μs	FIFO empty
Delay, OR low to data out	t_{DH}	50	85		ns	SO = low
Min. reset pulse width	t_{MRW}		20	50	ns	
Delay, data out to OR high	t_{DA}	0	35		ns	SO = high
Input capacitance	CI			7	pF	Any pin



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
═	MUST BE STEADY	WILL BE STEADY
\\\\\\\\	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
////	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
XXXX	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig.3 Timing diagram

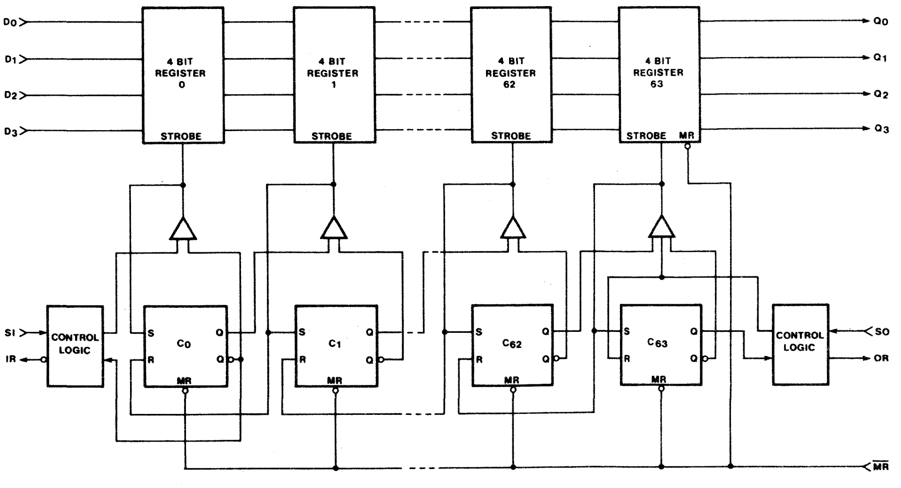


Fig.4 Logic block diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.
3. If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.

PLESSEY Semiconductors **ADVANCE INFORMATION CMOS**

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV21SC14

1024 x 4 BIT STATIC RAM

The MV21SC14 is a high speed, low power 4096-bit Static Random Access Memory, organised as 1024 words by 4-bits and fabricated with the ISO-CMOS process. It is a fully static device requiring neither clocks nor refresh circuitry. Bus-oriented systems are easily configured utilising its common I/O with 3-state outputs.

Whilst CS is high (Logic '1') and all inputs are within 200mV of Vss or Vcc the device remains in a low power standby mode, with Icc typically 10uA and data retained with Vcc down to 2V.

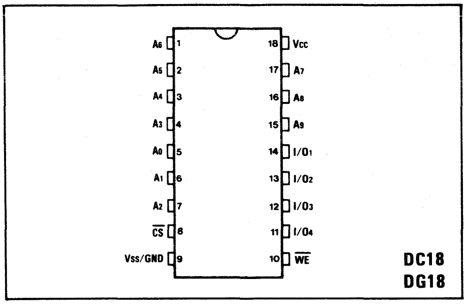


Fig.1 Pin connections (top view)

FEATURES

- Replacement for 2114L,2148,µPD444
- Fast Access Time (200-300ns)
- Fully Static Memory - no Clock or Strobe
- Low Operating Power (100mW)
- Low Standby Power (30µW)
- Common I/O with 3-State Outputs
- Fully TTL-Compatible
- 2V Standby Operation for Battery Backup
- Operating Voltage Range 3V to 7V
- Supplied in 18-pin Ceramic DIL (DG) and Ceramic Sidebrazed DIL (DC) packages
- Speed Selections: 300ns(-1) 250ns(-2) 200ns(-3)

PIN NAMES

A_0-A_9	Address inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
Vcc	Positive supply
Vss/GND	Ground

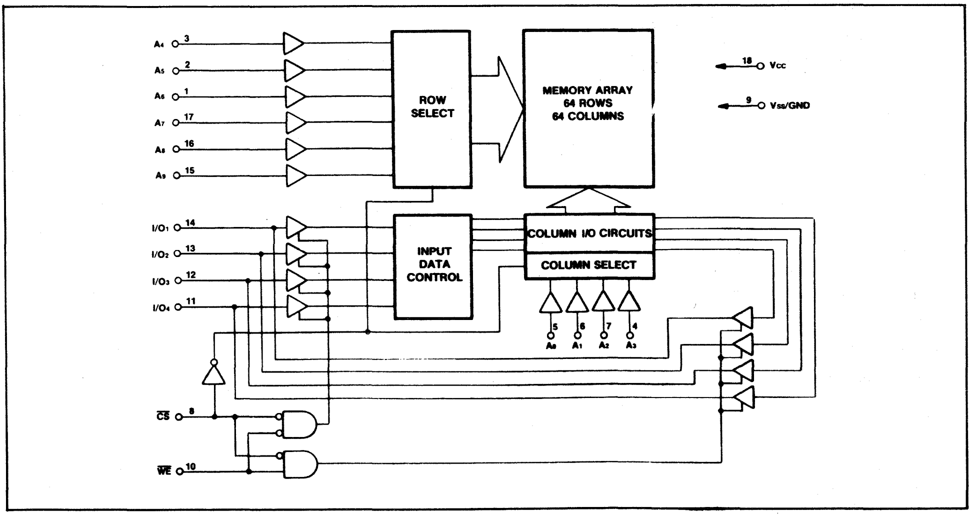


Fig.2 Block diagram

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	3	5	7	V
High level output current	I_{OH}		-10		mA
Low level output current	I_{OL}		10		mA
Operating free-air temperature	T_{amb}	0		70	°C

Note 1. Voltage values are with respect to Vss/GND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = +4.75V to +5.25V

Characteristic	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Operating supply voltage range	V_{CC}	3.0	5.0	7.0	V	
Standby supply voltage range	V_{CC}	2.0		7.0	V	
Operating supply current	I_{CC}		24		mA	$\overline{CS} = V_{IL}$, $V_{IN} = V_{IH}$, outputs O/C
Average operating supply current	I_{CCA}		10		mA	V_{IN} = GND or V_{CC}, f = 2MHz, duty 50%
Standby supply current	I_{CCS}		10		µA	$\overline{CS} = V_{CC}$, V_{IN} = GND or V_{CC}
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}			0.8	V	
High level output voltage	V_{OH}	2.4			V	I_{OH} = -400µA
Low level output voltage	V_{OL}			0.4	V	I_{OL} = 2.0mA
Input leakage current	I_{LI}	-10		10	µA	V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}	-10		10	µA	$\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}
Input capacitance	C_{IN}		5		pF	V_{IN} = 0V, f = 1MHz
Output capacitance	C_{OUT}		10		pF	V_{OUT} = 0V, f = 1MHz

Note 2. All Typical values at T_{amb} = 25°C, V_{CC} = 5V.

SWITCHING CHARACTERISTICS

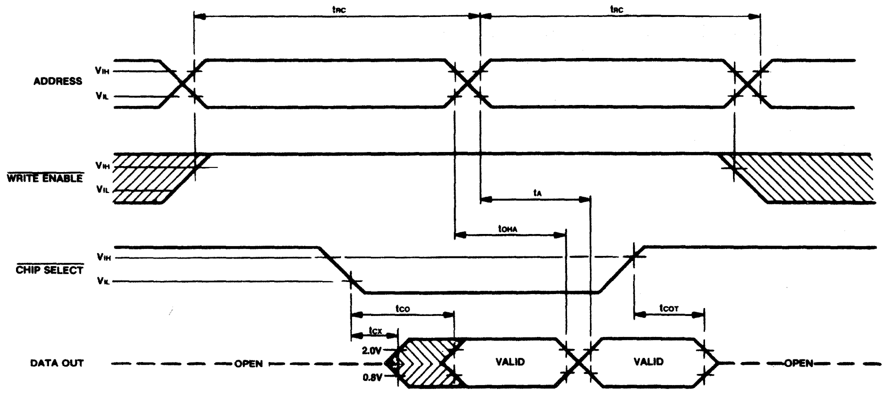
Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V, Output Load = 1 TTL gate and 100pF

Characteristic	Symbol	MV21SC14-1		MV21SC14-2		MV21SC14-3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
Read cycle time ($\overline{WE} = V_{IH}$)	t_{RC}	300		250		200		ns
Access time	t_A		300		250		200	ns
Chip Select to Output Valid	t_{CO}		300		250		200	ns
Chip Select to Output Active	t_{CX}	20		20		20		ns
Chip Select to Output Three-State	t_{COT}		80		70		60	ns
Output Hold from Address Change	t_{OHA}	50		40		30		ns
Write Cycle								
Write cycle time	t_{WC}	300		250		200		ns
Address to Write Set-up time	t_{AW}	0		0		0		ns
Write pulse width	t_{WP}	230		210		180		ns
Write recovery time	t_{WR}	0		0		0		ns
Data Set-up time	t_{DS}	150		140		120		ns
Data Hold time	t_{DH}	0		0		0		ns
Write Enable to Output Three-State	t_{WOT}		80		70		60	ns

ABSOLUTE MAXIMUM RATINGS

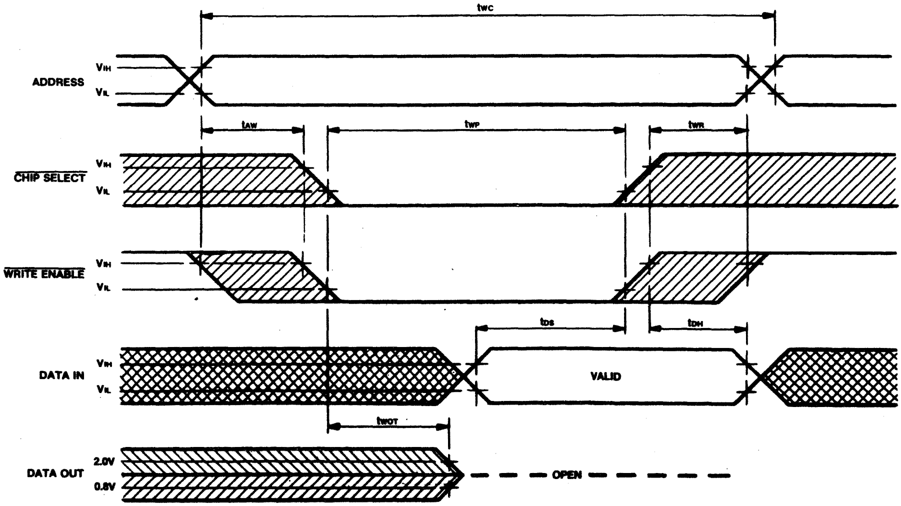
The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_I	-0.3 to V_{CC} + 0.3	V
Output current per O/P	I_O	±20	mA
Storage temperature	T_S	-65 to 150	°C
Operating temperature	T_{amb}	-40 to +85	°C
Package power dissipation	P	450	mW



Note: Input levels 0.4V to 3.0V.
Input rise/fall times 10ns.

Fig.3 Switching time waveforms - Read cycle



Note: Input levels 0.4V to 3.0V.
Input rise/fall times 10ns.

Fig.4 Switching time waveforms - Write cycle

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MV23SC16

2048 x 8 ROM

The MV23SC16 is a high speed, low power 16384-bit Static Read-Only Memory, organised 2048 words by 8-bits and fabricated with the ISO-CMOS process.

A manufacturing mask stage, defined by the user, programs the 16384-bit non-volatile memory array and true/inverse polarity on each of the three chip select inputs CS1, CS2 and CS3. Bus-oriented systems are easily configured using the three-state outputs. In system development a standard EPROM (eg 2716) may be used and subsequently replaced by the MV23SC16 to minimise power supply requirements and production costs.

FEATURES

- Pin-Compatible with 2316/2716
- Fast Access Time (350ns)
- Fully Static - no Clock or Strobe
- Low Operating Power (100mW)
- Low Standby Power (100µW)
- Three Programmable Chip Selects
- Three-State Outputs
- Fully TTL-Compatible
- Operating Voltage Range 3V to 7V
- Supplied in 24-pin Ceramic DIL (DG) Package

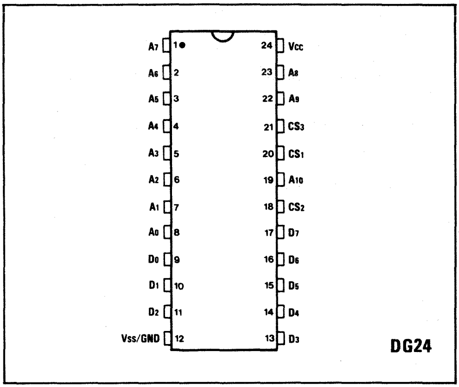

Fig.1 Pin connections (top view)

PIN NAMES

A_0-A_{10}	Address inputs
D_0-D_7	Data outputs
CS_1-CS_3	Programmable chip select inputs
V_{CC}	Positive supply voltage
V_{SS}/GND	Ground

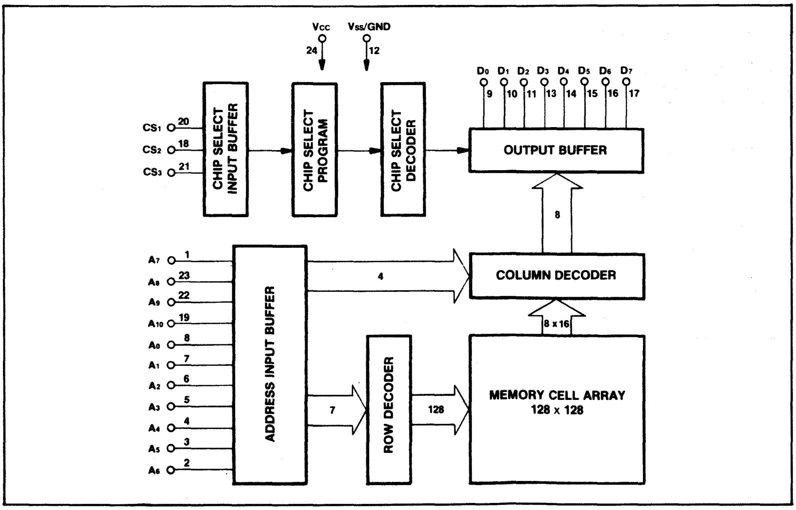

Fig.2 Block diagram

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	3	5	7	V
High level output current	I_{OH}		-10		mA
Low level output current	I_{OL}		10		mA
Operating free-air temperature	T_{amb}	0		70	°C

Note 1. Voltage values are with respect to Vss/GND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = +4.75V to +5.25V

Characteristic	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Operating supply voltage range	V_{CC}	3.0	5.0	7.0	V	
Operating supply current	I_{CC}		24		mA	$V_{IN} = V_{IH}$ or V_{IL}, outputs O/C
Average operating supply current	I_{CCA}		10		mA	V_{IN} = GND or V_{CC}, f = 1MHz, duty 50%
Standby supply current	I_{CCS}		20		µA	Deselected, V_{IN} = GND or V_{CC}
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}			0.8	V	
High level output voltage	V_{OH}	2.4			V	I_{OH} = -400µA
Low level output voltage	V_{OL}			0.4	V	I_{OL} = 2.0mA
Input leakage current	I_{LI}	-10		10	µA	V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}	-10		10	µA	Deselected, V_{OUT} = GND to V_{CC}
Input capacitance	C_{IN}		5		pF	V_{IN} = 0V, f = 1MHz
Output capacitance	C_{OUT}		10		pF	V_{OUT} = 0V, f = 1MHz

Note 2. All Typical values at T_{amb} = 25°C, V_{CC} = 5V.

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V, Output Load = 1 TTL Gate and 100pF

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Chip Select access time	t_{CS}			150	ns
Data Hold time from Deselect	t_{DF}	10		100	ns
Address access time	t_A			350	ns
Data Hold time from address change	t_{DH}	10			ns

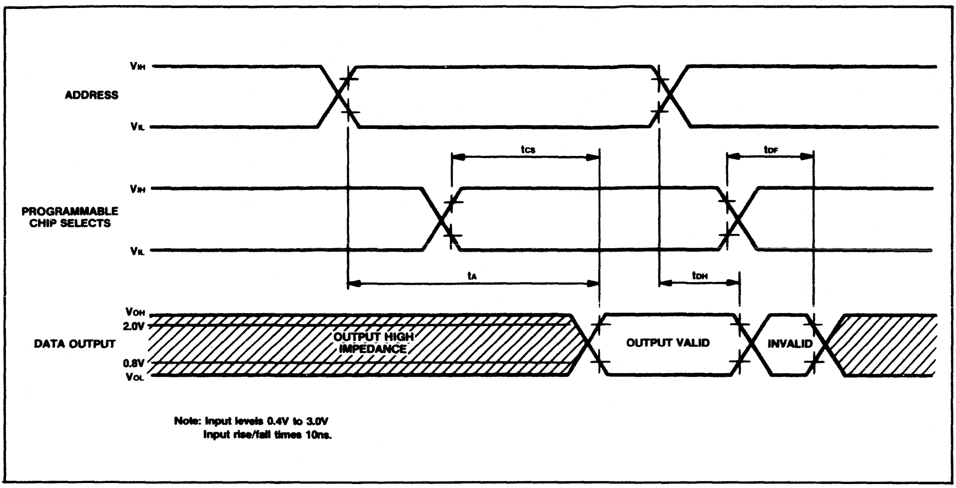

Fig.3 Switching time waveforms

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_I	-0.3 to V_{CC} + 0.3	V
Output current per O/P	I_O	±20	mA
Storage temperature	T_S	-65 to 150	°C
Operating temperature	T_{amb}	-40 to +85	°C
Package power dissipation	P	450	mW

CUSTOM PROGRAMMING

Both the 16384-bit ROM content and the Active Logic Polarity for each of Chip Selects CS1, CS2 and CS3 must be specified during manufacture of the MV23SC16 ROM.

Customer Definition of ROM Content

Plessey Semiconductors prefers the following:

(a) Customer-programmed 2K x 8 EPROM/EEPROM 24 pin devices, supplied in duplicate. (eg 2516, 2716, 48016, 2816)
(b) 2316 ROM device
(c) As (a) but unambiguously labelled pairs of 1K x 8 devices. (eg 2708, 2758, 3008, 27C58)

The following is also acceptable:

Magnetic Tape - 9 track 800 or 1600 bpi with data in the Motorola/AMI ASCII Hexadecimal Record (S-code) format. Maximum byte count per record of nineteen (hex 13), corresponding to a maximum of sixteen (hex 10) data bytes per record, is preferred, but not essential.

Customer Definition of Chip Select Polarity

The customer should specify, by letter carrying authorising signature and management function, or on an official purchase order, the following:

Pin Number	20	18	21
CHIP SELECT	CS1	CS2	CS3
Active HIGH or LOW with respect to V_{SS}/GND			

Plessey Semiconductors will add a unique suffix to the MV23SC16 designation when coding the packaged device, eg MV23SC16-012

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MV41SC04

QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

The MV41SC04 Quad Low Voltage to High Voltage Translator with 3-state outputs is designed to interface low voltage circuits to high voltage circuits, such as 5 Volt CMOS, NMOS or TTL to 12 Volt CMOS. It provides 4 Data Inputs (I_0-I_3), an active HIGH Output Enable Input (OE), 4 Data Outputs (Z_0-Z_3) and their complements ($\overline{Z_0}$-$\overline{Z_3}$). With the Enable HIGH, the Outputs are either HIGH or LOW as determined by the Data inputs; with the Output enable LOW, all the Outputs are in the high impedance 'OFF' state.

The device uses a common negative supply (V_{SS}) and separate positive supplies, inputs (V_{DDI}) and output (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. The input signals may be driven from any potential between V_{DDO} and V_{SS} without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10mA.

When used in a bus organized system all MV41SC04 devices on the same bus line should be connected to the same V_{DDO} and V_{SS} supplies.

The device is available in the 16-pin ceramic DIL (DG) package.

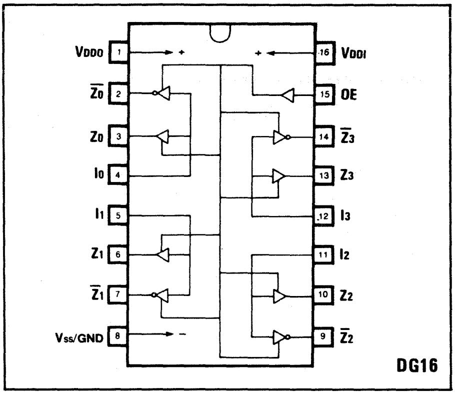

Fig.1 Pin connections (top view)

FEATURES

- ■ Pin-for-Pin Compatible with Fairchild F4104/34104
- ■ No Latch-up Problems
- ■ 3-State Fully Buffered Outputs
- ■ Bus-Orientated Translator/Drivers
- ■ Dual Power Supply Inputs
- ■ High Speed Performance

Pin Names	Function
I_0-I_3	Data Inputs
OE	Active HIGH enable
Z_0-Z_3	3-State data outputs
$\overline{Z_0}$-$\overline{Z_3}$	3-State complementary data outputs
V_{DDO},V_{DDI}	Positive supply voltages
V_{SS}/GND	System ground

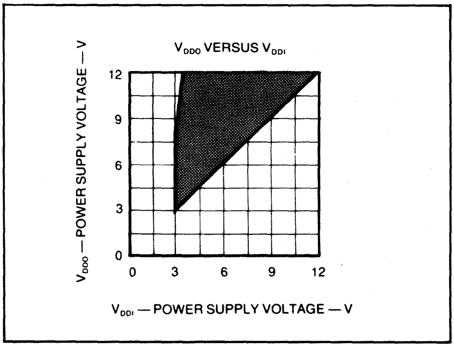

Fig.2 Typical supply voltage region of operation

RECOMMENDED OPERATING CONDITIONS

All voltages are with respect to V_{SS}/GND.

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{DDO}	3		12	V
Supply voltage	V_{DDI}	3		V_{DDO}	V
Low level output current	I_{OL}		24		mA
High level output current	I_{OH}		-24		mA
Operating temperature	T_{amb}	0		70	°C

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DDO} = V_{DDI}$ as shown, V_{SS}/GND = 0V
T_{amb} MIN = 0°C T_{amb} MAX = +70°C

SYMBOL	PARAMETER	LIMIT						UNIT	TEMP T_{amb}	TEST CONDITIONS
		$V_{DDO/I}=5$ V			$V_{DDO/I}=10$V					
		MIN	TYP	MAX	MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage	3.5		*	7.0		*	V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	**		1.5	**		3.0	V	All	Guaranteed Input LOW voltage
V_{OH}	Output HIGH Voltage	4.99 4.95			9.99 9.95			V	MIN, 25°C MAX	$I_{OH}=0$ mA Note 1
		4.0			9.0				All	$I_{OH}=0$ mA Note 2
V_{OL}	Output LOW Voltage			0.01 0.05			0.01 0.05	V	MIN, 25°C MAX	$I_{OL}=0$ mA Note 1
				0.5			1.0		All	$I_{OL}=0$ mA Note 2
I_I	Input Current			0.1			0.1	µA	25°C	Lead Under Test at 0 V or V_{DDO}. All Other Inputs Simultaneously at 0 V or V_{DDO}
I_{OH}	Output HIGH Current	−1.5 −1.0						mA	MIN, 25°C MAX	$V_{OUT}=2.5$ V for $V_{DDO}=5$V Note 1
		−0.7 −0.4			−1.4 −0.8				MIN, 25°C MAX	$V_{OUT}=V_{DDO}-0.5$ V Note 2
I_{OL}	Output LOW Current	1.0 0.8 0.4			2.6 2.0 1.2			mA	MIN 25°C MAX	$V_{OUT}=0.4$ V for $V_{DDO}=5$ V $V_{OUT}=0.5$ V for $V_{DDO}=10$ V Note 1
I_{OZH} Note 3	Output OFF Current HIGH			0.5 30			1.0 60	µA	MIN, 25°C MAX	Output Returned to V_{DDO}, OE=V_{SS}
I_{OZL} Note 3	Output OFF Current LOW			-0.5 -30			-1.0 -60	µA	MIN, 25°C MAX	Output Returned to V_{SS}, OE=V_{SS}
I_{DD}	Quiescent Power Supply Current			50 700			100 1400	µA	MIN, 25°C MAX	All Inputs Common and at 0 V or V_{DDI}

*V_{IH} must be less than or equal to V_{DDO}. If V_{IH} is greater than V_{DDO}, current at each input must be limited to 10 mA.
**V_{IL} must be greater than or equal to V_{SS}. If V_{IL} is less than V_{SS}, current at each input must be limited to 10 mA.
Notes:
1. Inputs at 0 V or V_{DDO} per function.
2. Inputs at 0.3 V_{DDO} or 0.7 V_{DD} per function.

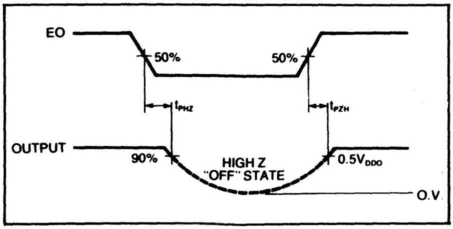

Fig.3 Output enable time (T_{pZH}) and output disable time (t_{pHZ})

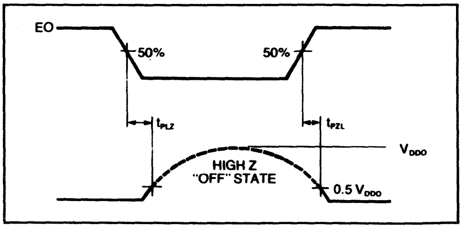

Fig.4 Output enable time (t_{pZL}) and output disable time (t_{pLZ})

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DDI} = 5V$, V_{DDO} as shown, $T_{amb} = 25°C$

SYMBOL	PARAMETER	LIMIT						UNIT	TEST CONDITIONS
		V_{DDO}=5 V			V_{DDO}=10 V				
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay.		135			75		ns	C_L=15 pF
t_{PHL}	I_n to Z_n or $\bar{Z}_n$		135			75		ns	Input Transition Times < 20 ns
t_{PZH}	Output Enable		190			95		ns	R_L=1 kΩ to V_{ss}
t_{PZL}	Time		185			90		ns	R_L=1 kΩ to V_{DDO}
t_{PHZ}	Output Disable		100			75		ns	R_L=1 kΩ to V_{ss}
t_{PLZ}	Time		100			70		ns	R_L=1 kΩ to V_{DDO}
t_{TLH}	Output Transition		30			18		ns	
t_{THL}	Time		30			18		ns	
t_{PLH}	Propagation Delay.		160			85		ns	C_L=50 pF
t_{PHL}	I_n to Z_n or $\bar{Z}_n$		160			85		ns	Input Transition Times < 20 ns
t_{PZH}	Output Enable		200			100		ns	R_L=1 kΩ to V_{ss}
t_{PZL}	Time		200			100		ns	R_L=1 kΩ to V_{DDO}
t_{PHZ}	Output Disable		115			80		ns	R_L = 1kΩ to V_{SS}
t_{PLZ}	Time		110			80		ns	R_L=1 kΩ to V_{DDO}
t_{TLH}	Output Transition		60			30		ns	
t_{THL}	Time		60			30		ns	

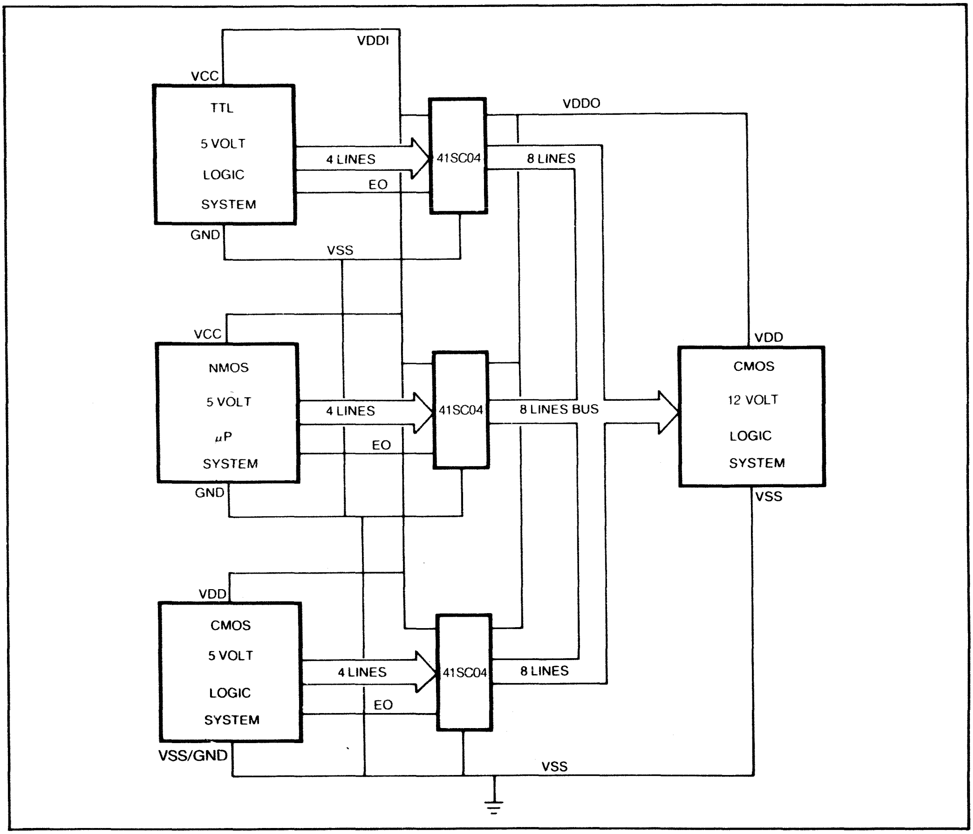

Fig.5 MV41SC04 typical application block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DDO} : -0.5V to 12V
Supply voltage, V_{DDI} : $-0.5V \leqslant V_{DDO}$
Voltage at any input, V_{IN} : -0.3V to V_{DDO} + 0.3V
Current into any input, I_{IN} : ±10mA
Operating temperature, T_{amb} : -40 to +85°C
Storage temperature, T_{stg} : -65 to +150°C

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MV4311 MV4368 MV4511

LATCHED 7-SEGMENT DECODER/DRIVERS

The MV4311, MV4368 and MV4511 are latched 7-Segment Decoder/Drivers fabricated with the Metal Gate CMOS Process and feature Bipolar NPN output stages sourcing well in excess of 20mA per segment output. Therefore current limiting resistors (e.g. 150-270 ohms) should be utilised when direct driving LED displays.

Latches on the four Address (Data) inputs (A,B,C,D) are controlled by Latch Enable (LE). When LE is low the output state is determined by the input data (Fallthrough). When LE is taken high that data at the inputs satisfying the setup time is stored in the latches and the outputs remain stable (Latch enabled). The high impedance of the data inputs permits direct multiplexed drive from MOS devices without need for additional drivers.

The MV4511 contains a BCD-to-7-segment decoder which blanks the outputs (all low) on input codes 10 through 15. The MV4311 and MV4368 contain a Hexadecimal-to-7-segment decoder producing numeric output 0 through 9 and alpha output, using mixed upper and lower case, A through F, as shown in Fig. 2.

The MV4311 and MV4511 also include Lamp Test ($\overline{LT}$) and Blanking ($\overline{BI}$) inputs used respectively to test the display, or turn off or pulse modulate the display brightness. On the MV4368 these inputs are replaced by $\overline{RBI}$ and $\overline{RBO}$, providing automatic blanking of leading or trailing zeroes in a multidigit display. An example of leading zero suppression is shown in Fig. 8(a), and trailing zero suppression in Fig. 8(b). The $\overline{RBO}$ pin can also be wired-ORed with the output of a suitable buffer to realise pulse modulation of display brightness, as shown in Fig. 7.

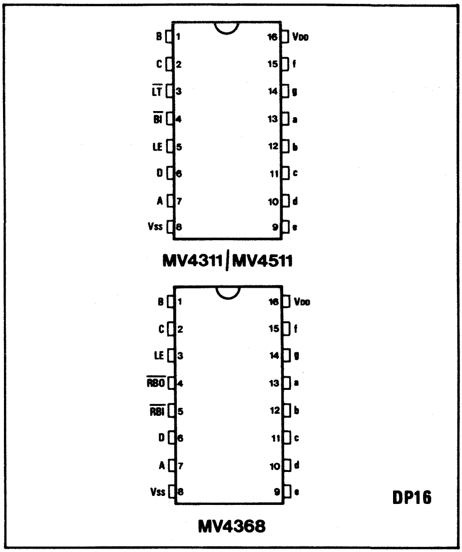


Fig.1 Connection diagrams (top view)

FEATURES

- MV4511 Compatible with 14511/4511
- MV4311 Provides 4511 Features with Hex Output
- MV4368 Second Source to TTL 9368
- Pinouts Comparable with many other Devices
- 3V to 18V Operation
- High Speed Input Latches
- Hexadecimal Decoding (MV4311/MV4368)
- Cascadable Ripple Blanking (MV4368)
- Guaranteed 20mA Output
- Supplied in 16 Pin DIL Plastic (DP) Package

PIN NAMES

A,B,C,D	Address (Data) inputs
LE	Latch Enable input
$\overline{BI}$	Blanking Input
$\overline{LT}$	Lamp Test input
$\overline{RBI}$	Ripple Blanking Input
$\overline{RBO}$	Ripple Blanking Output
a,b,c,d,e,f,g	Segment outputs
V_{DD}	Positive supply
V_{SS}	Ground

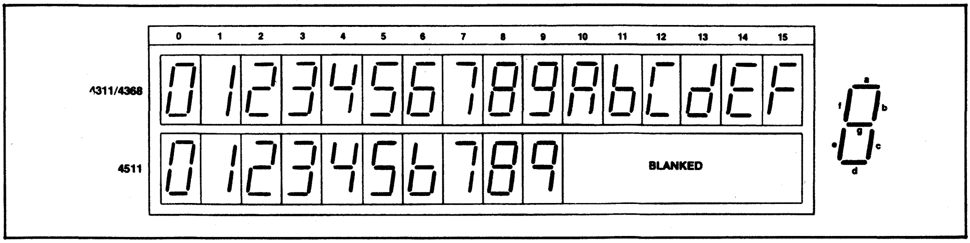


Fig.2 Display formats

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, typ. values at T_{amb} = +25°C

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Input high voltage	V_{IH}	5.0	3.5	2.75		V	V_O = 1.5V or 3.5V
		10.0	7.0	5.50		V	V_O = 3.0V or 7.0V
		15.0		8.25		V	V_O = 4.5V or 10.5V
Input low voltage	V_{IL}	5.0		2.25	1.5	V	V_O = 1.5V or 3.5V
		10.0		4.50	3.0	V	V_O = 3.0V or 7.0V
		15.0		6.75		V	V_O = 4.5V or 10.5V
Input leakage current	I_{IN}				±1.0	μA	V_{IN} = V_{SS} to V_{DD}
Output low $\overline{RBO}$	V_{OL}	5.0		0.25	0.4	V	I_{OL} = 0.4mA
		10.0			0.5	V	I_{OL} = 0.8mA
		15.0			1.5	V	I_{OL} = 2.4mA
Output high $\overline{RBO}$	V_{OH}	5.0	4.5			V	I_{OH} = -150μA
		10.0	9.5			V	I_{OH} = -350μA
		15.0	13.5			V	I_{OH} = -1100μA
Output drive voltage segment outputs	V_{OH}	5.0	4.00	4.57		V	I_{OH} = 0mA
			3.50	4.12		V	I_{OH} = -10mA
			2.80	3.75		V	I_{OH} = -20mA
		10.0	9.00	9.56		V	I_{OH} = 0mA
			8.65	9.17		V	I_{OH} = -10mA
			8.10	8.90		V	I_{OH} = -20mA
		15.0		14.59		V	I_{OH} = 0mA
				14.18		V	I_{OH} = -10mA
			13.10	13.95		V	I_{OH} = -20mA
Output drive voltage segment outputs	V_{OL}	5.0			0.4	V	$\|I_{OL}\|$ = 0.35mA
		10.0			0.5	V	$\|I_{OL}$ = 0.90mA
		15.0			1.5	V	$\|I_{OL}$ = 2.4mA
Quiescent current	I_{DD}	5.0			150	μA	All inputs at V_{SS} or V_{DD}
		10.0			300	μA	
		15.0			600	μA	

SWITCHING CHARACTERISTICS (Fig. 6)

Test conditions (unless otherwise stated):
T_{amb} = 25°C, C_L = 50pF

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Output rise time	t_r	5.0		40	250	ns	
		10.0		30	160	ns	
		15.0		18		ns	
Output fall time	t_f	5.0		200		ns	
		10.0		160		ns	
		15.0		100		ns	
Data propagation delay time	t_{pLH}	5.0		640	2250	ns	
		10.0		250	900	ns	
		15.0		175			
	t_{pHL}	5.0		720	2250	ns	
		10.0		290	900	ns	
		15.0		195		ns	
Blank propagation delay time	t_{pLH}	5.0		320	1500	ns	
		10.0		130	600	ns	
		15.0		100		ns	
	t_{pHL}	5.0		485	1500	ns	
		10.0		200	600	ns	
		15.0		160		ns	
Lamp test propagation delay time	t_{pLH}	5.0		290	940	ns	
		10.0		125	375	ns	
		15.0		85		ns	
	t_{pHL}	5.0		290	940	ns	
		10.0		120	375	ns	
		15.0		90		ns	

SWITCHING CHARACTERISTICS (CONT.)

Characteristic	Symbol	V_{DD}(V)	Value			Unit	Conditions
			Min.	Typ.	Max.		
Setup time	t_{SETUP}	5.0	270	90		ns	
		10.0	114	38		ns	
		15.0		20		ns	
Hold time	t_{HOLD}	5.0	0	-90		ns	
		10.0	0	-38		ns	
		15.0		-20		ns	
Latch enable pulse width	PW_{LE}	5.0	780	260		ns	
		10.0	330	110		ns	
		15.0		65		ns	

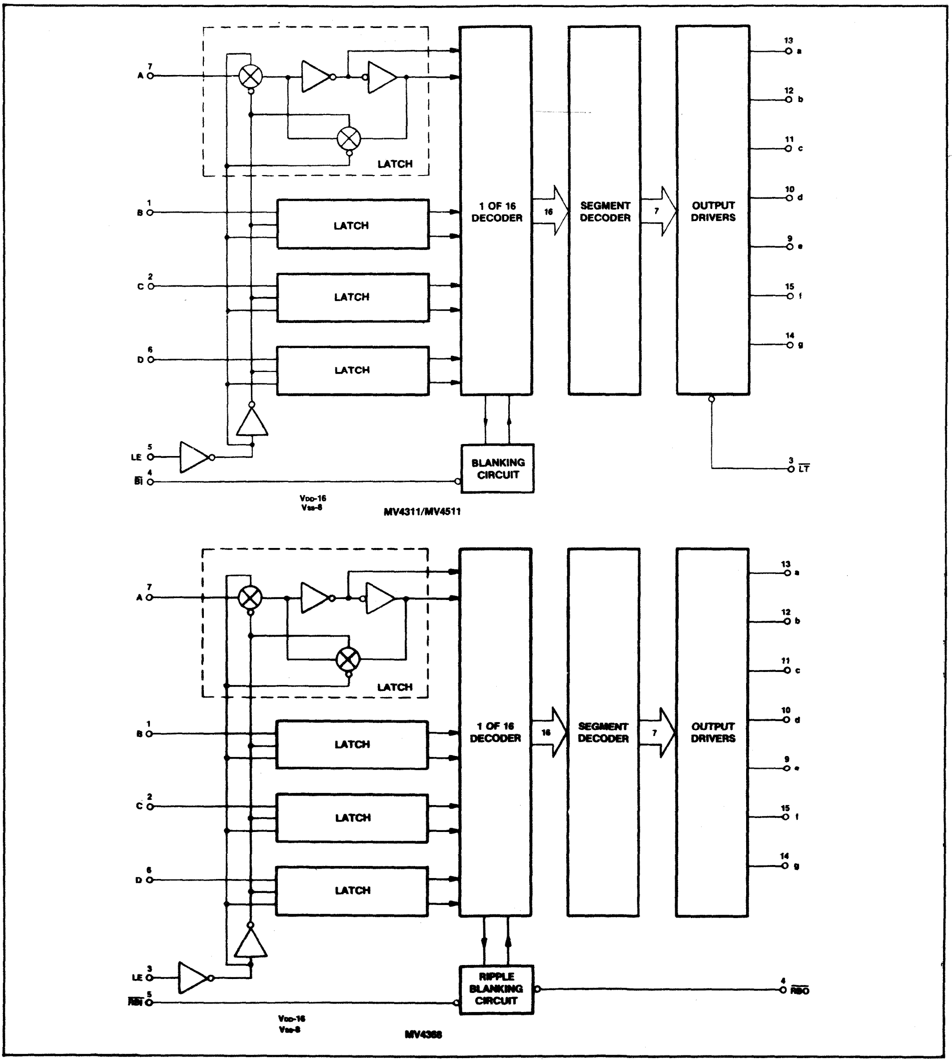
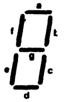


Fig.3 Block diagrams

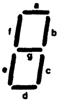
Inputs							MV4311 Outputs							Display	MV4511 Outputs							Display
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g		a	b	c	d	e	f	g	
H	H	H	X	X	X	X	STABLE							STABLE	STABLE							STABLE
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK	L	L	L	L	L	L	L	BLANK
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8	H	H	H	H	H	H	H	8
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	H	L	H	H	H	H	H	6	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	H	L	H	H	9	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	H	H	H	L	H	H	H	A	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	H	H	H	H	H	b	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	H	L	L	H	H	H	L	C	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	H	H	H	H	L	H	d	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	H	L	L	H	H	H	H	E	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	H	L	L	L	H	H	H	F	L	L	L	L	L	L	L	BLANK



Definition	Inputs	Outputs
H	HIGH voltage level	Sourcing current
L	LOW voltage level	Output is 'off'
X	Don't care	

Fig.4 MV4311 & MV4511 Truth tables

Inputs						MV4368 Outputs								Display
LE	$\overline{RBI}$	D	C	B	A	a	b	c	d	e	f	g	$\overline{RBO}$	
H	*	X	X	X	X	STABLE							H	STABLE
L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
L	X	L	L	L	H	L	H	H	L	L	L	L	↓	1
L	↓	L	L	H	L	H	H	L	H	H	L	H		2
L		L	L	H	H	H	H	H	H	L	L	H		3
L		L	H	L	L	L	H	H	L	L	H	H		4
L		L	H	L	H	H	L	H	H	L	H	H		5
L		L	H	H	L	H	L	H	H	H	H	H		6
L		L	H	H	H	H	H	H	L	L	L	L		7
L		H	L	L	L	H	H	H	H	H	H	H		8
L		H	L	L	H	H	H	H	H	L	H	H		9
L		H	L	H	L	H	H	H	L	H	H	H		A
L		H	L	H	H	L	L	H	H	H	H	H		b
L		H	H	L	L	H	L	L	H	H	H	L		C
L		H	H	L	H	L	H	H	H	H	L	H		d
L		H	H	H	L	H	L	L	H	H	H	H		E
L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK



* $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

** $\overline{RBO}$ used as an input overrides all other input conditions.

Definition	Inputs	Outputs
H	HIGH voltage level	Sourcing current
L	LOW voltage level	Output is 'off'
X	Don't care	

Fig.5 MV4368 Truth table

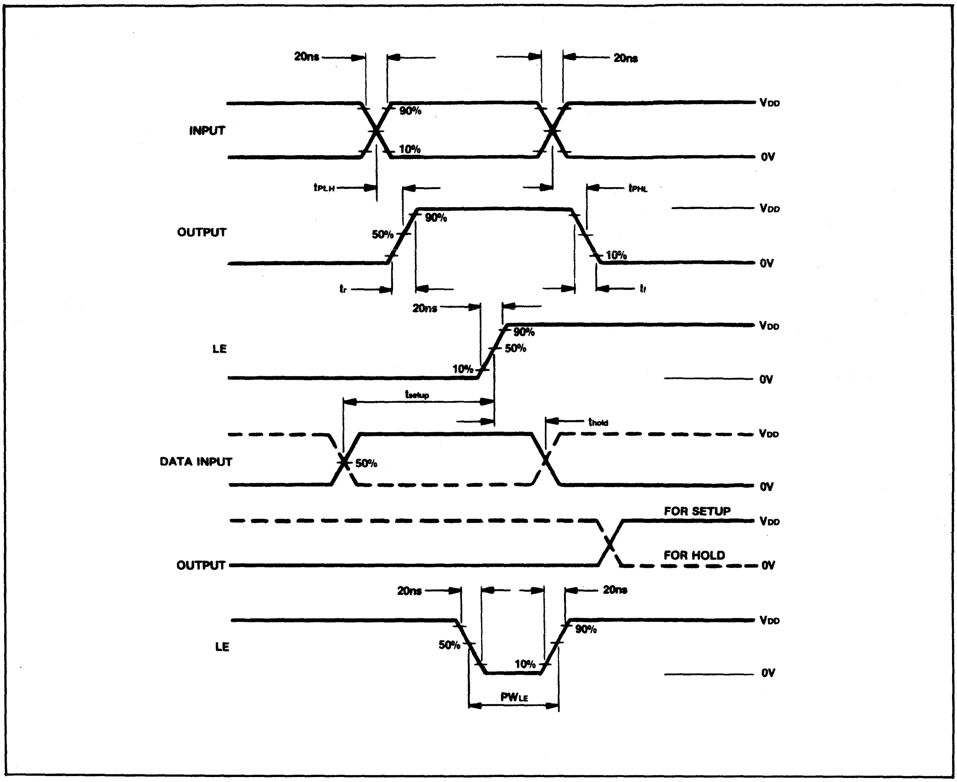
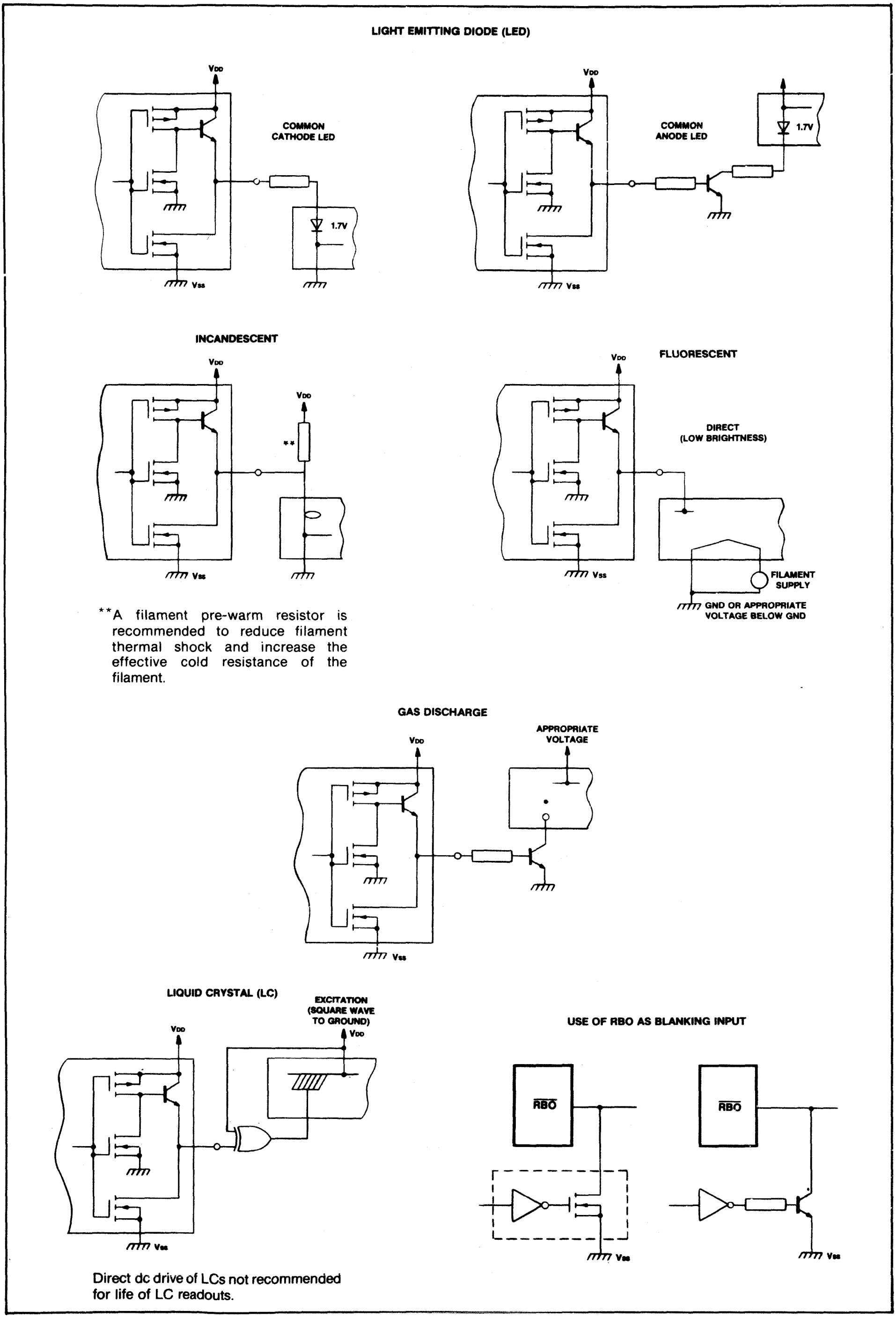


Fig.6 Timing waveforms

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded. All voltages with respect to Vss.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{DD}	-0.5 to 18	V
Input voltage	V_I	-0.5 to V_{DD} +0.5	V
Maximum continuous output source current, per output	I_{OH} max.	30	mA
Maximum continuous power dissipation per output	P_{OH} max.	50	mW
Storage Temperature range	T_S	-65 to +125	°C
Operating temperature range	T_{amb}	0 to +70	°C


LIGHT EMITTING DIODE (LED)

INCANDESCENT

FLUORESCENT

GAS DISCHARGE

LIQUID CRYSTAL (LC)

USE OF RBO AS BLANKING INPUT

**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCs not recommended for life of LC readouts.

Fig.7 Examples of connection to various display types.

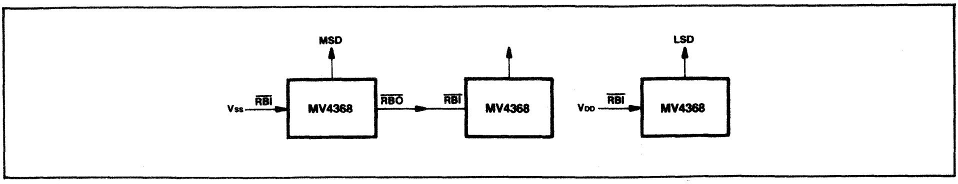


Fig.8(a) Leading zero suppression (A zero on least significant digit will not be suppressed if connected as shown)

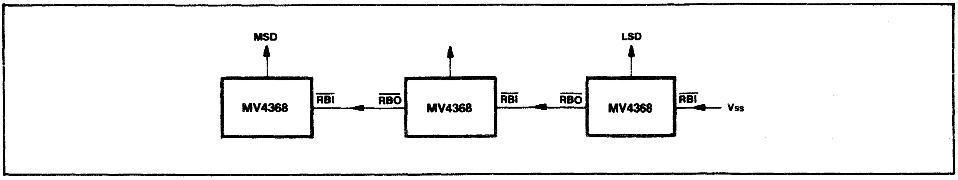


Fig.8(b) Trailing zero suppression

PLESSEY
Semiconductors

ADVANCE INFORMATION CMOS

MV4320/MV4322/MV4323

KEYPAD PULSE DIALLER

The MV4320 series is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and offers a REDIAL option activated by key #. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing mark/space ratio and dialling speed are pin selectable.

The MV4322 and MV4323 provide the same function as the MV4320, except the MV4322 provides the M2 muting function in place of M1 and the MV4323 provides "Inter Digit Pause" (IDP) selection in place of Mark/Space (M/S) ratio selection.

The MV4320, MV4322 and MV4323 are available in Ceramic DIL (DG, -40°C to +85°C).

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 932 Hz
- Low Cost

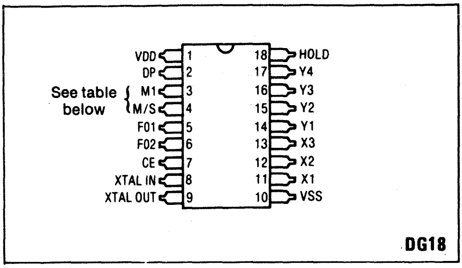


Fig.1 Pin connections (top view)

Type No.	Pin 3	Pin 4
MV4320	M1	M/S
MV4322	M2	M/S
MV4323	M1	IDP

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

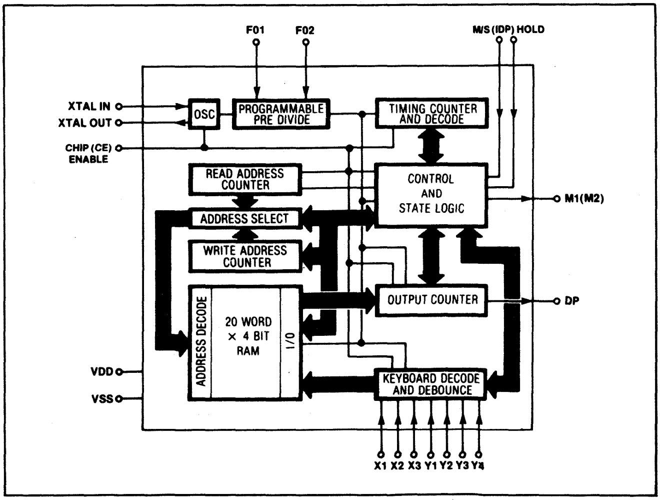


Fig.2 MV4320/MV4322/MV4323 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	μA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	200	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-8.0	μA	$V_{IN} = V_{SS}$	X_1,X_2,X_3 Y_1,Y_2,Y_3,Y_4
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S,IDP,F01, F02,FD,HOLD
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$	
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	DP, M1/M2
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

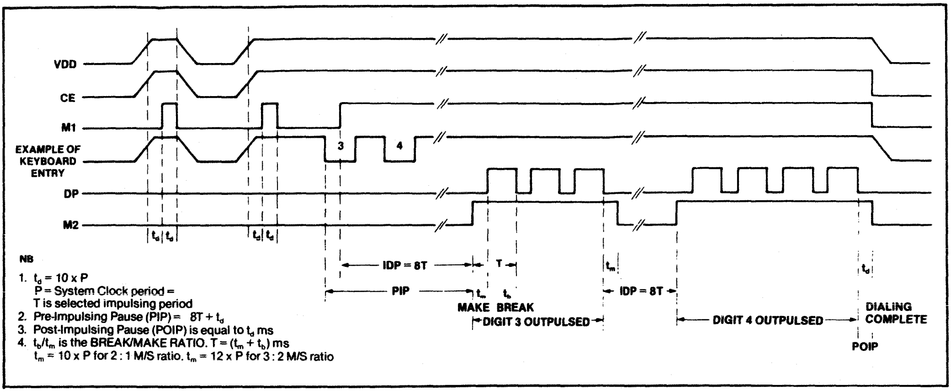
		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP,M_1.
15		Output Fall Time	t_F		1.0		us	C_L = 50pF
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

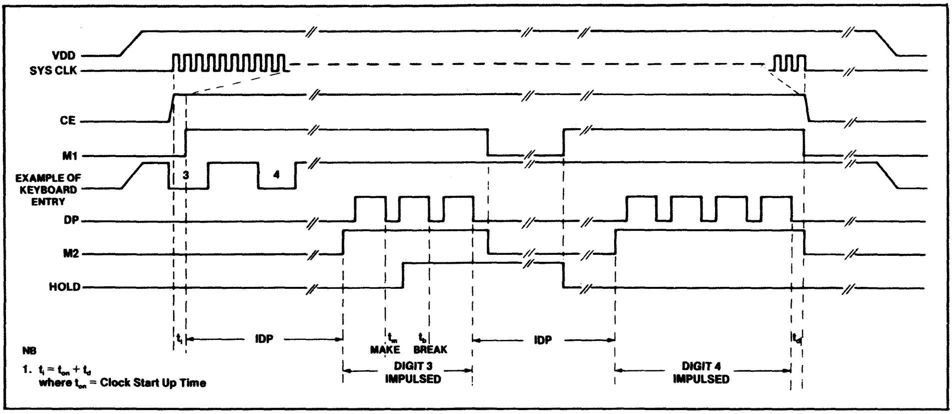
The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.



NB

1. $t_d = 10 \times P$
   P = System Clock period =
   T is selected impulsing period
2. Pre-Impulsing Pause (PIP) = $8T + t_d$
3. Post-Impulsing Pause (POIP) is equal to t_d ms
4. t_b/t_m is the BREAK/MAKE RATIO. $T = (t_m + t_b)$ ms
   $t_m = 10 \times P$ for 2 : 1 M/S ratio. $t_m = 12 \times P$ for 3 : 2 M/S ratio

Fig.3 Keypad pulse dialer timing diagram, CE-External control



NB

1. $t_i = t_{on} + t_d$
   where t_{on} = Clock Start Up Time

Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	$V_{SS}-0.3V$	$V_{DD}+0.3V$
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

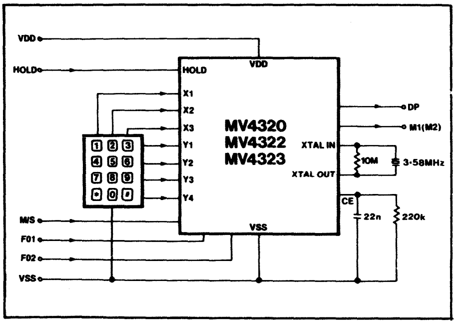


Fig.5 Application diagram

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="3">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="3">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1/M2</td><td colspan="3">Mute Output (Off Normal) Buffer</td></tr>
<tr><td rowspan="2">M/S</td><td rowspan="2">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C</td><td>2:1</td></tr>
<tr><td>V_{DD}</td><td>3:2</td></tr>
<tr><td rowspan="2">IDP</td><td rowspan="2">Inter-Digit Pause Select Note: T = Selected Impulsing Period</td><td>O/C</td><td>8T</td></tr>
<tr><td>V_{DD}</td><td>4T</td></tr>
<tr><td>F01,F02</td><td colspan="3">Impulsing Rate Selection.
On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.
<table>
<tr><th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Inpulsing Rate</th><th>System Clock frequency</th></tr>
<tr><td>O/C</td><td>O/C</td><td>10Hz</td><td>10.13Hz</td><td>303.9Hz</td></tr>
<tr><td>O/C</td><td>V_{DD}</td><td>20Hz</td><td>19.42Hz</td><td>582.6Hz</td></tr>
<tr><td>V_{DD}</td><td>O/C</td><td>932Hz</td><td>932.17Hz</td><td>27,965.1Hz</td></tr>
<tr><td>V_{DD}</td><td>V_{DD}</td><td>16Hz</td><td>15.54Hz</td><td>466.1Hz</td></tr>
</table></td></tr>
<tr><td>CE</td><td colspan="3">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="3">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="3">Crystal Output Buffer to drive crystal.</td></tr>
<tr><td>V_{SS}</td><td colspan="3">System ground</td></tr>
<tr><td>X_1, X_2, X_3</td><td colspan="3">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>Y_1, Y_2, Y_3, Y_4</td><td colspan="3">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td rowspan="3">HOLD</td><td></td><td>O/C</td><td>Normal Operation</td></tr>
<tr><td></td><td>V_{DD}</td><td>No impulsing. If activated during impulsing, hold occurs when the current digit is complete</td></tr>
<tr><td colspan="3">Prevents further impulsing. On-chip pull-down transistor to V_{SS}.</td></tr>
</table>

PLESSEY Semiconductors

ADVANCE INFORMATION CMOS

MV4325/MV4326

PROGRAMMABLE KEYPAD PULSE DIALLER

The MV4325 Keypad Pulse Dialler contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MV4325 has programmable access pause capability to provide automatic interruption of dialling needed when accessing the toll network, WATS line or public network. The device is fabricated using Plessey Semiconductors' ISO-CMOS technology which enables the device to function down to 2.0V making it ideal for long loop operation.

The MV4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1μA at 1.0V.

The MV4326 provides the same function as the MV4325 except that the M2 muting function is provided instead of M1 offered in the MV4325.

The MV4325 and MV4326 are available in Ceramic DIL (DG, -40°C to +85°C).

APPLICATIONS

- Pushbutton Telephones with Last Number Redial
- Repertory Dialers
- Tone to Pulse Converters

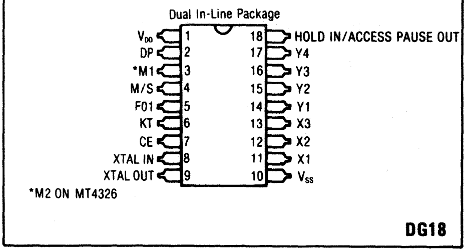


Fig.1 Pin connections (top view)

FEATURES

- Last Number Redial
- Multiple Access Pause Programming
- Any Valid Keypad Input or HOLD IN Causes Exit from Access Pause
- Oscillator Start Up Controlled from Keypad Input
- Oscillator Power Down whilst not Dialling
- 300 Hz Key Tone indicates Valid Key
- 2.0V to 7.0V Supply Voltage Operating Range
- Stores up to 20 Digits and Access Pauses
- Digit Memory Retained down to 1.0V at 1μA
- Selectable Mark/Space Ratio 66⅔ : 33⅓ or 60 : 40
- 10 Hz Dialling Speed (14.9kHz Fast Test)

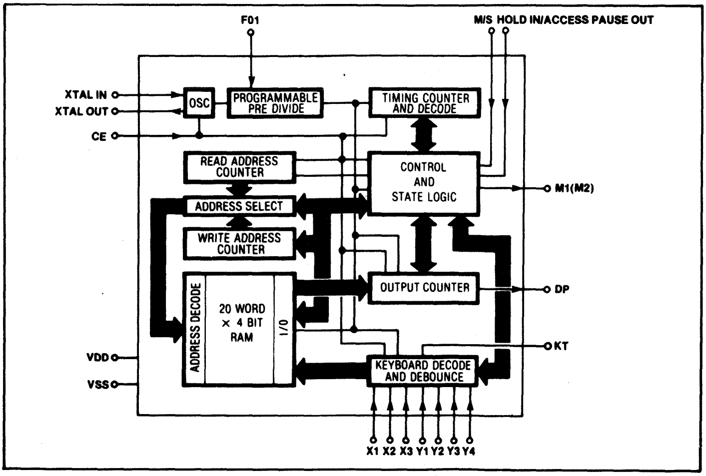


Fig.2 MV4325/MV4326 functional block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN	MAX		MIN	MAX
$V_{DD}-V_{SS}$	-0.3V	10V			
Voltage on any pin	V_{SS}-0.3V	$V_{DD}+0.3V$			
Current at any pin		10mA			
Operating Temperature	-40 °C	+85°C	Power Dissipation		1000mW
Storage Temperature	-65 °C	+ 150 °C			

* Derate 16mW/ °C above 75 °C. All leads soldered to PC board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $f_{CLK} = 3.579545 MHz$; $V_{DD} = +3.0V$
All voltages wrt V_{SS}

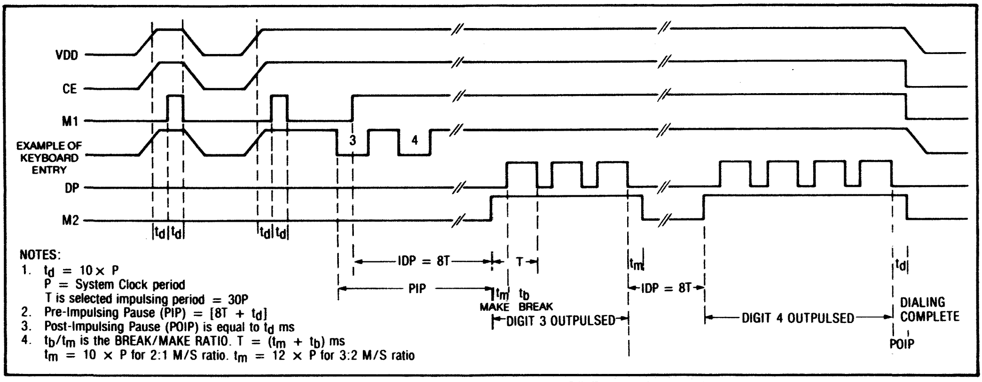
CHARACTERISTIC				SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2		Standby Supply Current		I_{DDS}			1.0	μA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.0V	
3		Operating Supply Current		I_{DD}		100	150	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	− 0.5	− 3.0	− 8.0	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		− 0.1		nA	$V_{IN} = V_{SS}$	M/S, F01
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$	
8		Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9		Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	DP, M_1, M_2, KT
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel	I_{OL}	0.8	2.0		mA	$V_{OUT} = 2.3V$	
13				I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	
14			P-Channel Source	I_{OH}	− 0.8	− 2.0		mA	$V_{OUT} = 0.7V$	
15				I_{OH}	− 0.2	− 0.5		mA	V_{OUT} = 2.5V	
16	IN/OUTPUT	Input Low Level Voltage		V_{IL}			0.9	V		
17		Input High Level Voltage		V_{IH}	2.1			V		
18		Output Low Level Current		I_{OL}		15		μA	V_{OUT} = 0.5V	CE,
19		Output High Level Current		I_{OH}		− 12		μA	V_{OUT} = 2.5V	HOLD IN/ACCESS
20		Input Force High Current (from V_{OL})		I_{FH}		55		μA	V_{IN} = 2.5V	PAUSE OUT
21		Input Force Low Current (from V_{OH})		I_{FL}		− 70		μA	V_{IN} = 0.5V	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC ELECTRICAL CHARACTERISTICS

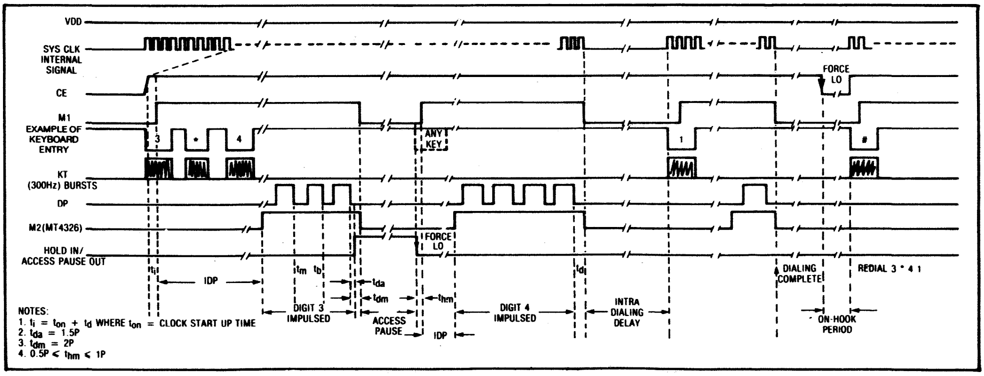
Test conditions (unless otherwise stated):
$T_{amb} = +25°C$; $f_{CLK} = 3.579545$ MHz; $V_{DD} = +3.0V$

		CHARACTERISTIC	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			14.9		kHz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input



NOTES:
1. $t_d = 10 \times P$
   P = System Clock period
   T is selected impulsing period = 30P
2. Pre-Impulsing Pause (PIP) = $[8T + t_d]$
3. Post-Impulsing Pause (POIP) is equal to t_d ms
4. t_b/t_m is the BREAK/MAKE RATIO. T = $(t_m + t_b)$ ms
   $t_m = 10 \times P$ for 2:1 M/S ratio. $t_m = 12 \times P$ for 3:2 M/S ratio

Fig.3 MV4325/MV4326 timing diagram, CE External control



NOTES:
1. $t_i = t_{on} + t_d$ WHERE t_{on} = CLOCK START UP TIME
2. $t_{da} = 1.5P$
3. $t_{dm} = 2P$
4. $0.5P \leqslant t_{hm} \leqslant 1P$

Fig.4 MV4325/MV4326 timing diagram, CE Internal control

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="5">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="5">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1 (M2)</td><td colspan="5">Mute Output Buffer</td></tr>
<tr><td rowspan="2">M/S</td><td colspan="3" rowspan="2">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C</td><td>2:1</td></tr>
<tr><td>V_{DD}</td><td>3:2</td></tr>
<tr><td rowspan="3">F01</td><td rowspan="3">Impulsing Rate Selection.
On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.</td><td>F01</td><td>Nominal Impulsing Rate</td><td>Actual* Inpulsing Rate</td><td>System Clock frequency</td></tr>
<tr><td>O/C</td><td>10Hz</td><td>10.13Hz</td><td>303.9Hz</td></tr>
<tr><td>V_{DD}</td><td>14.9kHz</td><td>14,915Hz</td><td>447.4kHz</td></tr>
<tr><td>CE</td><td colspan="5">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="5">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="5">Crystal Output. Buffer to drive crystal. Capacitive load on-chip.</td></tr>
<tr><td>V_{SS}</td><td colspan="5">System ground</td></tr>
<tr><td>X_1,X_2,X_3</td><td colspan="5">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.</td></tr>
<tr><td>Y_1,Y_2,Y_3,Y_4</td><td colspan="5">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.</td></tr>
<tr><td rowspan="3">HOLD IN/
ACCESS
PAUSE OUT</td><td>INPUT/OUTPUT</td><td>O/C</td><td colspan="3">Normal Operation</td></tr>
<tr><td>INPUT</td><td>V_{DD}</td><td colspan="3">No impulsing. If activated during impulsing, hold occurs when the current digit is complete.</td></tr>
<tr><td>OUTPUT</td><td>V_{DD}</td><td colspan="3">Logic "1" level output indicates access pause condition.</td></tr>
<tr><td>KT</td><td colspan="5">300Hz Square wave bursts indicate valid keypad input.</td></tr>
</table>

		KEYPAD INPUT CODE						
No. of O/P Pulses	**Digit**	**Y_1**	**Y_2**	**Y_3**	**Y_4**	**X_1**	**X_2**	**X_3**
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0
ACCESS PAUSE		1	1	1	0	0	1	1

Table 1

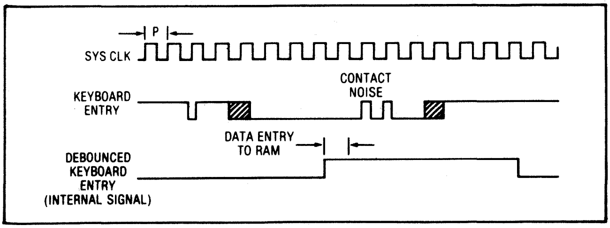


Fig.5 Keypad input debounce timing diagram

OPERATING NOTES

The MV4325 programmable keypad pulse dialer is optimized for use in key operated pulse dialling telephone sets and contains features which make it particularly suitable for applications where redial of last number dialled and repertory dial facilities are required.

Keypad information is accepted directly from a dual contact keypad having two single pole switches per key: one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 1.

The MV4325 will accept up to 20 digits and access pauses, e.g. 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10ms is rejected and any input valid for greater than 17ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig.5.

The first key entered in any dialling sequence initiates the oscillator on the MV4325 by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in Fig.3 and Fig.4. Fig.3 shows use of the MV4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig.4 shows the timing diagram of the MV4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialling commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 (and M2 on the MV4326) goes low and Hold In/Access Pause Out goes high indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialling of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low, resetting the output latch associated with this input/output pin.

Fig.4 shows a pause in dialling between the completion of dialling digit 4 and keying digit 1. In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialling resumes.

The end of a key entry sequence is indicated to the MV4325 by externally pulsing or clamping CE low. This causes the on-chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialled will occur. Access pause operation is as previously described. In the standby condition the MV4325 dissipates less than 1.0μW.

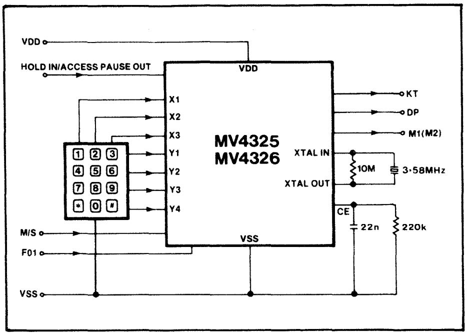


Fig.6 Application diagram

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MV4330 MV4331 MV4332

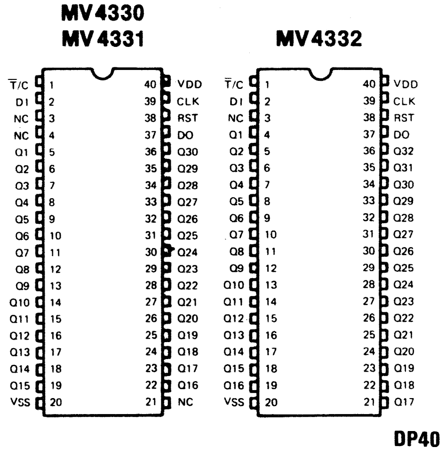
CMOS/LSI 30/32-BIT STATIC SHIFT REGISTERS WITH PARALLEL TRUE/COMPLEMENT OUTPUTS

The MV4330, 4331, and 4332 are CMOS/LSI 30 and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alpha-numeric displays plus decimal points or two 16-segment alpha-numeric displays directly.

The devices are available in 40-pin plastic DIL (DP) package.

FEATURES

- Direct LCD Drive
- CMOS Low Power (1 μA)
- 3 to 18 Volt Operation
- On-Chip Wave-Shaping
- High Speed (Typ. 3 MHz) Shift Register



PIN NAMES

DI	Serial Data Input
DO	Serial Data output
CLK	Clock (positive transition) input
RST	Master Reset (active HIGH) input
$\overline{\text{T}}$/C	True/Complement (active LOW) input
Q1 to Q32	True/Complement outputs

Fig.1 Pin connections (top view)

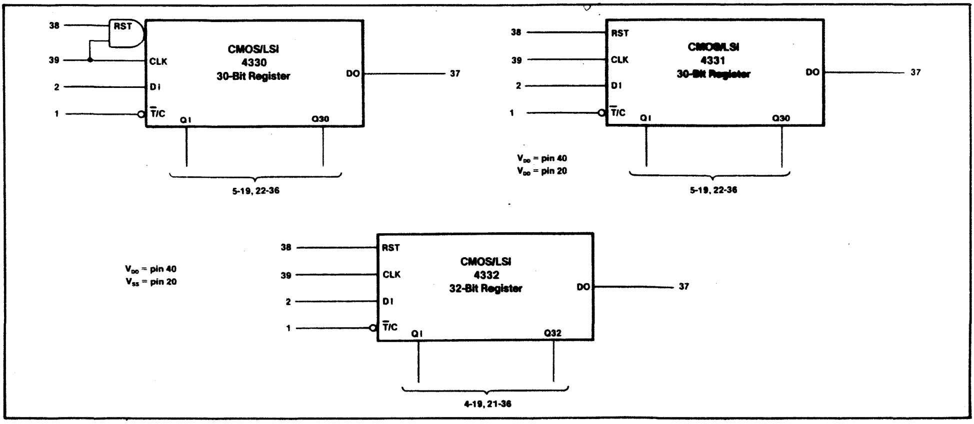


Fig.2 Block diagrams

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

CHARACTERISTIC		SYMBOL	TEST CONDITIONS			LIMIT			UNIT
				VO Volts	VDD Volts	Min.	Typ.	Max.	
Quiescent Device Current		I_L			5	–	0.5	50	uA
					10	–	1	100	
Output Voltage	Low-Level	VOL			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	VOH			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		VNL		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		VNH		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	IDN	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		IDP	P-Channel	4.5	5	−0.35	−0.9	–	
				9.5	10	−0.8	-1.9	–	
	Q OUT	IDN	N-Channel	0.5	10	50	250	–	uA
		IDP	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $C_L = 50pF$
All input rise and fall times = 20ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMIT			UNIT
			VDD Volts	Min.	Typ.	Max.	
Propagation Delay Time	tPHL tPLH		10	–	300	–	ns
Transition Time	tTHL	D OUT (CL=50pF)	10	–	70	130	ns
	tTLH	Q OUT (CL=15pF)	10	–	300	–	ns
Maximum Clock Frequency	fCL		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	tWL tWH		10	–	200	–	ns
Minimum Reset Pulse Width	tWH(R)		10	–	200	–	ns
Input Capacitance	CI	Any Input		–	5	–	pF

Note 1.Voltages with respect to V_{ss}
Note 2.Typical temperature coefficient for all values = 0.3%/°C

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	LIMIT	UNIT
DC Supply Voltage	VDD	-0.5 to 18	V
Input Voltage	VIN	-0.5 to VDD+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Ts	-65 to 125	°C

OPERATING NOTES

The MV4330, MV4331 and MV4332 accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these devices is that the clock input and the true/complement control (T/C) input have wave-shaping circuits (Fig.3) to ensure fast edges on-chip regardless of the shape of the incoming signals.

The MV4330 also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The MV4331 and MV4332 have asynchronous reset (RST) inputs which are active HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (DO) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

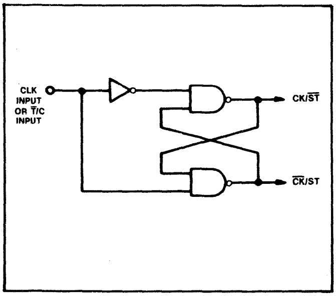


Fig.3 Wave shaping circuit

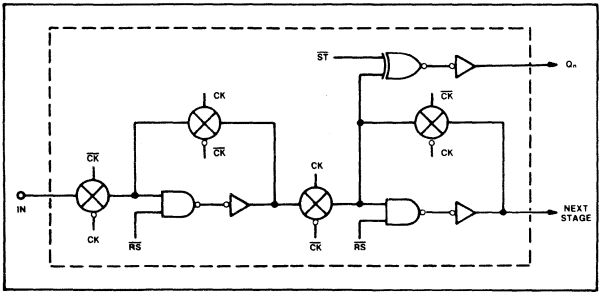


Fig.4 One stage of shift register

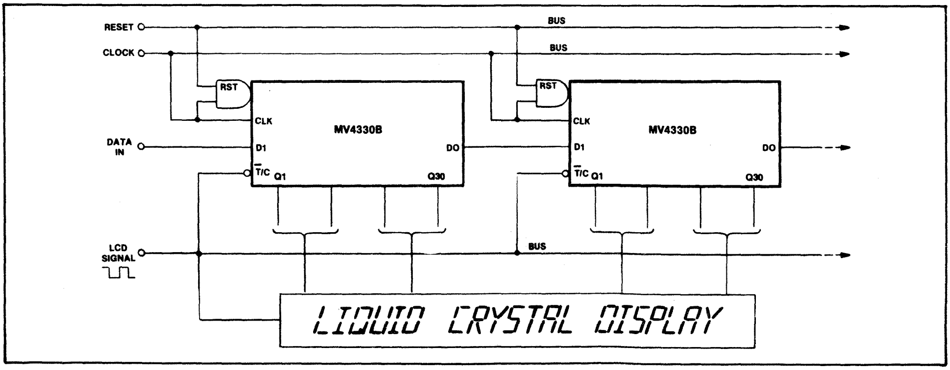


Fig.5 Typical application

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MV68SC02

8-BIT MICROPROCESSOR

The MV68SC02 is a monolithic 8-bit microprocessor fabricated with the high density, high speed ISO-CMOS process. It offers all registers and accumulators of the MC6800, **plus** on-chip oscillator and 128 bytes of static RAM located at hexadecimal addresses 0000 to 007F. The device requires only external CMOS ROM program memory (e.g. MV23SC16) to form a micropower microcomputer.

The device is fully software, function and pin-compatible with the MC6802. Operation is quasi-static in that the clock may be interrupted only with the E clock output (pin 37) in the high (logic '1') state. In this condition the low standby power dissipation is realised and all memory and register contents retained.

NB external addressed and enabled memory or peripherals must be static.

FEATURES

- Standby Power Dissipation 500μW
- Single Supply
- Operating Voltage Range 3V to 7V
- Standby Voltage Range 2V to 7V
- Software Compatible with MC6800
- Software, Function and Pin - Compatible with MC6802
- 128-Byte Static RAM and Oscillator On-Chip
- Operation DC to 2MHz (8MHz crystal)
- Operating Power Dissipation 75mW at 2MHz
- Fully TTL-Compatible
- All Memory and Registers Retainable in Standby Mode
- 16-bit Memory Addressing up to 65K Words
- Supplied in 40-pin Sidebrazed DIL (DC) package

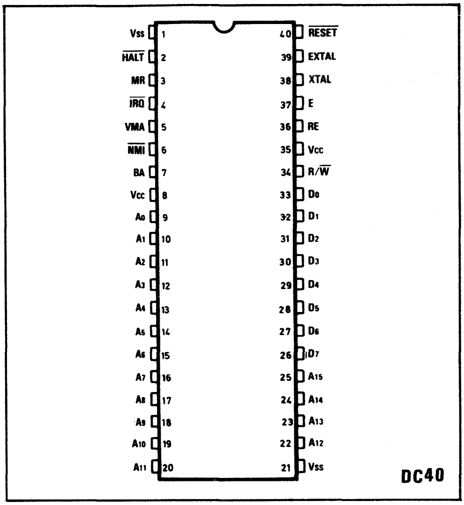

Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Limit	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_I	-0.3 to V_{CC} + 0.3	V
Output current	I_O	±20	mA
Storage temperature	T_S	-65 to 150	°C
Operating temperature	T_{amb}	-40 to 85	°C
Power dissipation	P	450	mW

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	3	5	7	V
High level, output current	I_{OH}		-10		mA
Low level, output current	I_{OL}		10		mA
Operating temperature	T_{amb}	0		70	°C

Note 1. Voltages are with respect to Vss

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V

Characteristic	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Operating supply voltage range	V_{CC}	3.0	5.0	7.0	V	
Standby supply voltage range	V_{CC}	2.0		7.0	V	
Standby supply current	I_{CCS}		100		µA	E = V_{OH}, V_{IN} = V_{SS} or V_{CC} EXTAL = V_{SS} or V_{CC}
Operating supply current	I_{CC}		15		mA	f = 2MHz
			3		mA	f = 1MHz
			300		µA	f = 100kHz
Read/Write protect threshold (RE - pin 36)			2.0		V	
Input high level voltage (except $\overline{RESET}$)	V_{IH}	2.0			V	
Input high level voltage $\overline{RESET}$	V_{IH}	4.0			V	
Input low level voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		10	µA	V_{IN} = V_{SS} to V_{CC}, Note 3
Output high level voltage						
D0-D7, E	V_{OH}	2.4			V	I_{OH} = -205uA
A0-A15,R/$\overline{W}$,VMA	V_{OH}	2.4			V	I_{OH} = -145uA
BA	V_{OH}	2.4			V	I_{OH} = -100uA
Output low level voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input capacitance D0-D7	C_{IN}		10		pF	V_{IN} = 0V, f = 1MHz
Logic inputs, EXTAL	C_{IN}		6		pF	
Output capacitance A0-A15, R/$\overline{W}$, VMA	C_{OUT}		10		pF	
Frequency of operation (EXTAL Clock ÷ 4)	f	0		2.0	MHz	f = 1/t_{CYC}
Crystal frequency	f_{XTAL}	0.20		8.0	MHz	
Clock cycle time	t_{CYC}	500			ns	Fig. 2 and Fig. 3
Clock pulse width	t_{ELO}	0.25		10	µs	Fig. 2 and Fig. 3
Instruction cycle time			2		µs	f = 2MHz
EXTAL clock rise and fall time	t_{OC}			25	ns	measured between 0.8V and 2.0V

Note 2. All Typical values at T_{amb} = 25°C, V_{CC} = 5V.
Note 3. Excluding EXTAL & XTAL.

SWITCHING CHARACTERISTICS(FIG.2 and FIG.3)

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = +4.75V to +5.25V, load circuit of Fig. 4

Characteristic	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Address delay	t_{AD}			160	ns	
Peripheral Read access time $t_{acc} = t_{CYC} - (t_f + t_{AD} + t_{DSR})$	t_{acc}			250	ns	t_{CYC} = 500ns
Data setup time (Read)	t_{DSR}	40			ns	
Input Data hold time	t_H	10			ns	
Output Data hold time	t_H	10			ns	
Address hold time (Address, R/$\overline{W}$, VMA)	t_{AH}	10			ns	
Data delay time (Write)	t_{DDW}			160	ns	
Processor controls						
Bus available delay	t_{BA}			135	ns	
Processor control setup time	t_{PCS}	125			ns	
Processor control rise and fall time	t_{PCr},t_{PCf}			100	ns	measured between 0.8V and 2.0V
Output rise and fall times	t_r,t_f			50	ns	measured between 0.4V and 2.4V

Note 4. 'Measured between 0.8V and 2.0V' applies only to t_{PCr} and t_{PCf}.

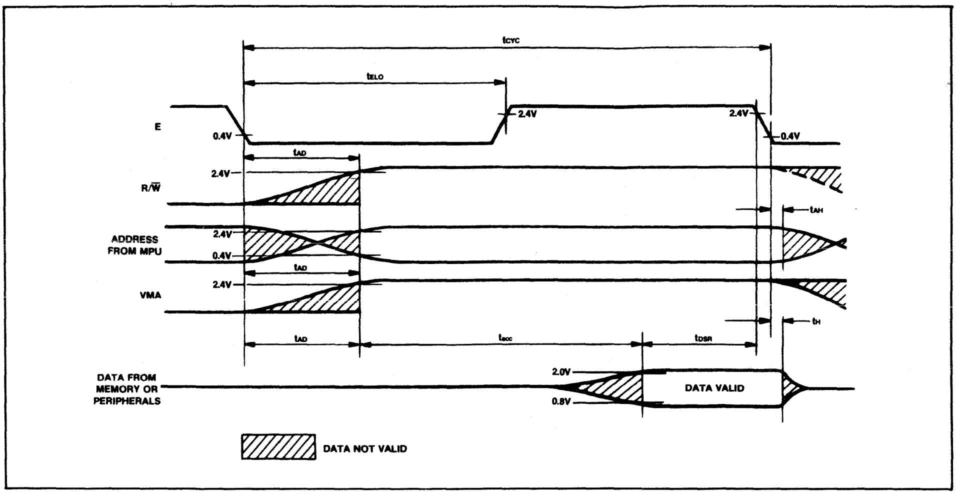

Fig.2 Read Data from Memory (or peripherals) timing

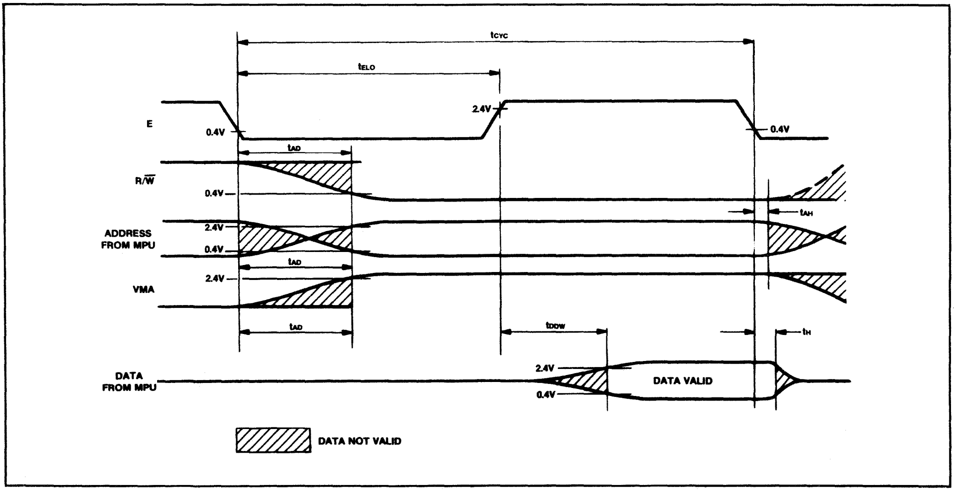

Fig.3 Write Data to Memory (or peripherals) timing

C = 130pF for D0-D7, E
= 90pF for A0-A15, $R/\overline{W}$, and VMA
= 30pF for BA
R = 11.7kohms for D0-D7, E
= 16.5kohms for A0-A15, $R/\overline{W}$ and VMA
= 24kohms for BA

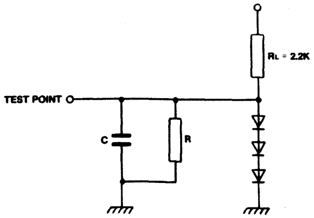

Fig.4 Load circuit for Address, Data, E, $R/\overline{W}$, VMA and BA

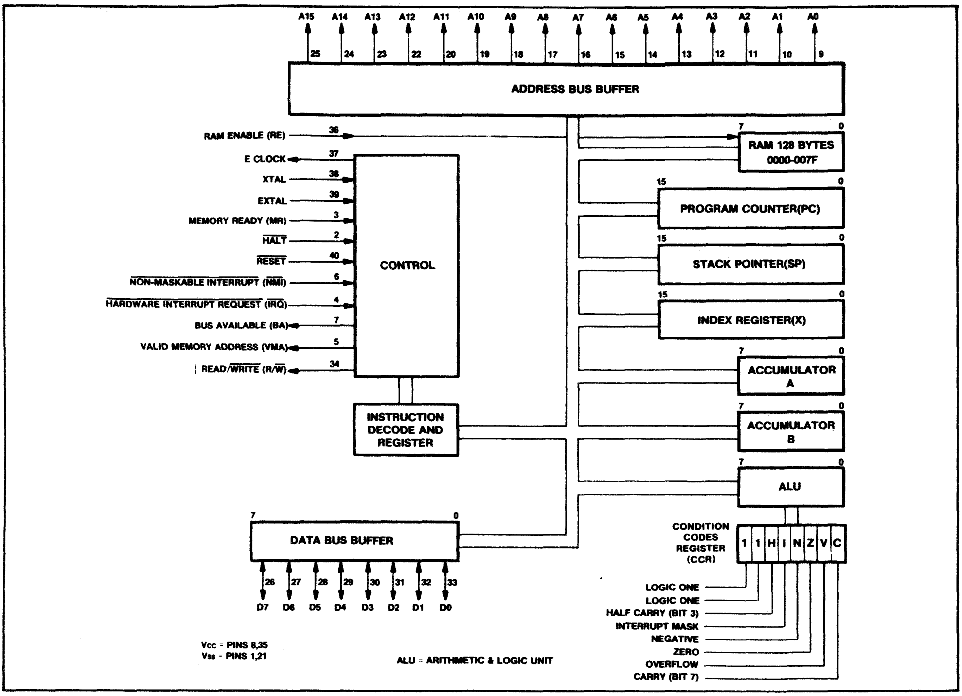

Fig.5 MV68SC02 block diagram and programming model

MV68SC02 SIGNAL DESCRIPTION

Proper operation of the MV68SC02 microprocessor requires that certain timing and control signals be provided and that other control signals be monitored to determine the state of the processor. The following is a summary of the 36 processor signals, (refer Block Diagram Fig. 5).

Address Bus (A0-A15) Sixteen pins each connected to a three-state bus driver capable of driving one standard TTL load and 90pF.

Data Bus (D0-D7) Eight pins each connected to a three-state bidirectional bus driver capable of driving one standard TTL load and 130pF.

Read/Write (R/W) This output indicates to memory (or peripheral) devices that the processor is in a Read (high or Logic '1') or Write (low or Logic '0') state. The normal state of this signal, including when the processor is halted or waiting for an interrupt following a WAI instruction, is high. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA) This output indicates to memory (or peripheral) devices that there is a valid address at the address outputs, and is capable of driving one standard TTL load and 90pF. When the processor is halted, or following a WAI instruction, this signal is low ('0' state).

Bus Available (BA) This output indicates that the processor has stopped and the address and data buses are available, e.g.when halted or following a WAI instruction. This output is capable of driving one standard TTL load and 30pF.

E Clock (E) This output is equivalent to ϕ2 on the MC6800 and is a single phase clock to the memory (or peripheral) devices capable of driving one standard TTL load and 130pF.

EXTAL and XTAL These two connections are for a parallel resonance fundamental crystal of AT cut and frequency four times the desired operating frequency. Alternatively EXTAL may be driven from an external TTL source with XTAL left open circuit. (In either case, the t_{ELO} limits must be met.) The low to high transition at EXTAL clocks the internal divide by four and EXTAL may be stopped with E high to perform single cycle execution.

Memory Ready (MR) This TTL-compatible input signal allows stretching of any positive half-cycle of E (for interfacing with slow memories) when taken low immediately after the commencement of that half-cycle.

HALT This TTL-compatible input signal allows processor operation to be halted or single-instruction stepped. HALT transitions should occur t_{PCS} before the rising edge of E. When taken low the processor will stop at the end of the current instruction, with BA and R/W high, VMA low and the Address and Data outputs in their high impedance state. If then HALT is returned high for just one E clock cycle, the processor will execute its next instruction and stop again. Interrupts NMI and IRQ, provided their pulse width exceeds t_{CYC}, will be latched if received whilst halted, and acted upon one instruction after resumption.

RESET This input is used to reset and start the processor from a power down condition, or to reinitialise the processor at any time. At power-up, RESET must be held low for a minimum of 8 E clock cycles, or 20ms, whichever is the greater. When reinitialising, RESET must be low for a minimum of 3 E clock cycles. Once these conditions have been satisified, whilst RESET remains low VMA and BA will be low with R/W high and the Data outputs in their high impedance state. The Address outputs will be set to the first Reset Vector Address FFFE, and the internal registers cleared.

When RESET is returned high, the contents of both FFFE and the second reset vector FFFF are loaded to the Program

Counter to effect indirect addressing to the programmer's initialisation routine, and the Interrupt Mask (CCR Bit 4) is set. (This bit must then be cleared under program control before the processor can be interrupted by IRQ.)

Hardware Interrupt Request (IRQ) This TTL-compatible input requests that an interrupt sequence be generated within the processor, which will complete the current instruction before recognising the request, and then only begin an interrupt sequence if the interrupt mask (CCR Bit 4) is clear. The interrupt sequence comprises 12 E clock cycles in which the program counter, index register, accumulators and condition code register are stacked, the interrupt mask is set, and the program counter loaded from IRQ vectors FFF8 and FFF9. The processor will thus branch to the programmer's IRQ servicing routine, which will usually conclude with an RTI instruction to unstack the interrupted program's parameters and effect resumption of that program.

Non-Maskable Interrupt (NMI) This TTL-compatible input also requests that an interrupt sequence be generated within the processor, but is not subject to the interrupt mask. An interrupt sequence commences at the end of the current instruction, stacking the registers then setting the interrupt mask. In the 11th and 12th cycles the program counter is loaded from NMI vectors FFFC and FFFD.

Both IRQ and NMI inputs are sampled whilst E clock is high, and provided that t_{PCS} is met, will start their interrupt sequence when E falls at the end of the current instruction. When IRQ or NMI inputs are answering a WAI instruction, the interrupt sequence is only 4 cycles. Both inputs can accept pulse widths down to t_{CYC}, but if both occur together, or if NMI is received just before an IRQ-initiated sequence reaches its vector cycles (11th and 12th cycles), vectors FFFC and FFFD will be accessed because NMI is given priority. In such an event a pulsed IRQ input will be lost because the interrupt mask will now be set.

RAM Enable (RE) This TTL-compatible input disables the internal RAM when taken low. This is necessary when external memory between addresses 0000 and 007F is to be accessed since the data bus is fixed in output mode when accessing the internal memory.

MV68SC02 INSTRUCTION SET

The MV68SC02 has a set of 72 instructions, listed alphabetically in Table 1. These instructions are executed in six different address modes - implied (inherent), immediate, direct, extended, indexed and relative. Of the 256 possible 8-bit operation codes, 197 are assigned. The instruction set is as for the MC6800/MC6802. Plessey Semiconductors' MV68SC02 Microprocessor Handbook* includes full details of the address modes, instruction descriptions, execution times and cycle by cycle operation summaries.

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

Table 1 Instruction set - alphabetical listing

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*Available last quarter 1981

PLESSEY Semiconductors **ADVANCE INFORMATION CMOS**

MV74SC137, MV74SC138, MV74SC139
MV74SC237, MV74SC238, MV74SC239

OCTAL DECODERS/DEMULTIPLEXERS

This family of ISO-CMOS MSI circuits is designed for use in high speed memory and peripheral address decoding systems. MV74SC138 and MV74SC238 decode 3 binary inputs (A_0, A_1, A_2) to select one of eight mutually exclusive outputs ($O_0 - O_7$). Three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3), reduce the need for external gates in an expanded system. MV74SC137 and MV74SC237 feature additional latches on A_0, A_1 and A_2 for use in glitch free applications. When Latch Enable (LE) is LOW the device acts as MV74SC138. When LE is HIGH the address present at A_0 to A_2 is stored. A 1 of 32 decoder requires only four of these devices and one inverter. MV74SC139 and MV74SC239 feature two individual, two line (A_0, A_1) to four line ($O_0 - O_3$) decoders. Each decoder has an active LOW Enable ($\overline{E}$) which can also be used as a data input in a full four-minterm of two variables decode, as shown in Fig.8.

The devices are available in the 16-pin ceramic DIL (DG) package.

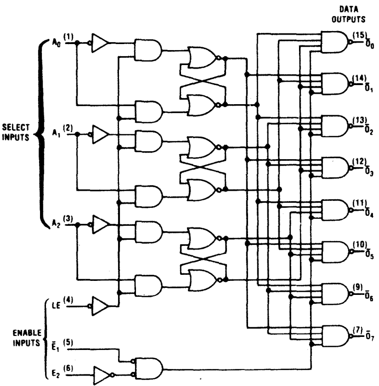
FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- High Current, Sink/Source Capability

DEVICE SELECTION

Product	Format	Output
MV74SC137	1 of 8, latched address	inverted
MV74SC138	1 of 8	inverted
MV74SC139	Dual 1 of 4	inverted
MV74SC237	1 of 8, latched address	non-inverted
MV74SC238	1 of 8	non-inverted
MV74SC239	Dual 1 of 4	non-inverted

FUNCTIONAL BLOCK DIAGRAMS AND LOGIC

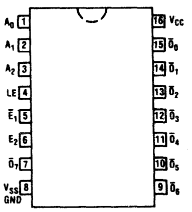


LOGIC DIAGRAM

INPUTS						OUTPUTS							
ENABLE			SELECT										
LE	E2	$\overline{E}_1$	A_2	A_1	A_0	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address. L: all others. H							

H = high level, L = low level, X = don't care

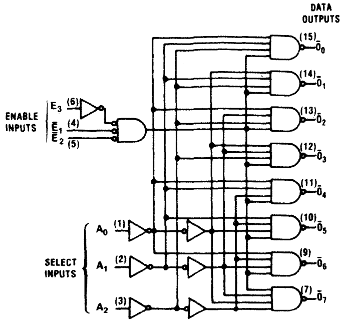
TRUTH TABLE



DG16

PIN CONNECTIONS (TOP VIEW)

Fig.1 MV74SC137

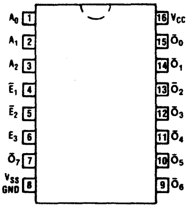


LOGIC DIAGRAM

INPUTS					OUTPUTS							
ENABLE		SELECT										
E_3	$\bar{E}_{1/2}$	A_2	A_1	A_0	$\bar{0}_0$	$\bar{0}_1$	$\bar{0}_2$	$\bar{0}_3$	$\bar{0}_4$	$\bar{0}_5$	$\bar{0}_6$	$\bar{0}_7$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = don't care

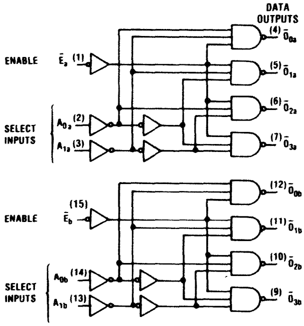
TRUTH TABLE



DG16

PIN CONNECTIONS (TOP VIEW)

Fig.2 MV74SC138

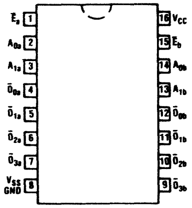


LOGIC DIAGRAM

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\bar{E}$	A_1	A_0	$\bar{0}_0$	$\bar{0}_1$	$\bar{0}_2$	$\bar{0}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

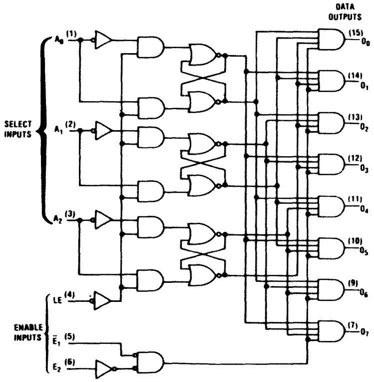
TRUTH TABLE (EACH HALF)



DG16

PIN CONNECTIONS (TOP VIEW)

Fig.3 MV74SC139

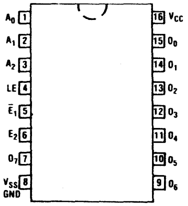


LOGIC DIAGRAM

INPUTS						OUTPUTS							
ENABLE			SELECT										
LE	E_2	$\bar{E}_1$	A_2	A_1	A_0	0_0	0_1	0_2	0_3	0_4	0_5	0_6	0_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address. H. all others. L							

H = high level, L = low level, X = don't care

TRUTH TABLE



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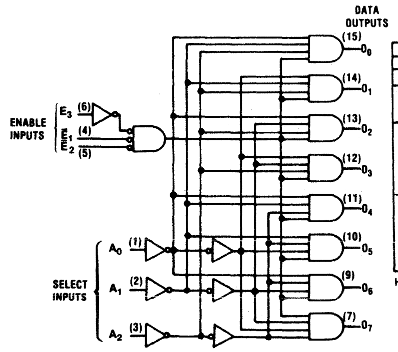
PIN CONNECTIONS (TOP VIEW)

Fig.4 MV74SC237

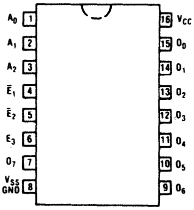


LOGIC DIAGRAM

INPUTS					OUTPUTS							
ENABLE		SELECT										
E_3	$\bar{E}_{1/2}$	A_2	A_1	A_0	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

H = high level, L = low level, X = don't care

TRUTH TABLE



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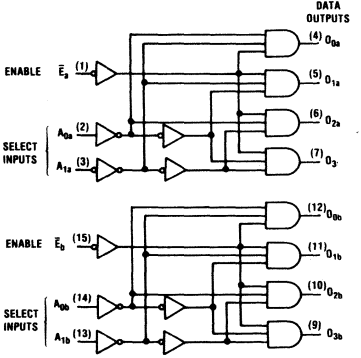
PIN CONNECTIONS (TOP VIEW)

Fig.5 MV74SC238

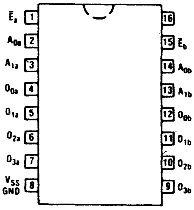


LOGIC DIAGRAM

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\bar{E}$	A_1	A_0	O_0	O_1	O_2	O_3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	L	H	L	H	L	L
L	H	L	L	L	H	L
L	H	H	L	L	L	H

H = high level, L = low level, X = don't care

TRUTH TABLE (EACH HALF)



DG16

PIN CONNECTIONS (TOP VIEW)

Fig.6 MV74SC239

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 0°C$ to $+70°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis (V_T+ − V_T-)		0.2	0.5		V	
High level output voltage	V_{OH}	2.4 4.35			V V	V_{CC} = 4.75V, I_{OH} = −14mA I_{OH} = −3mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 12mA
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			−10	µA	V_{CC} = 5.25V, V_I = 0.4V
Short circuit output current (2)	I_{OS}		−40		mA	V_{CC} = 5.25V
Supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs open

1. All TYP. values at T_{amb} = 25°C V_{CC} = 5V
2. Max. dissipation or 1 ms duration should not be exceeded.

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{CC} = 5V$, $T_{amb} = +25°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS C_L = 15pF, R_L = 2K
Propagation delay time Address to output	t_{PLH}		25		nS	
Propagation delay time Address to output	t_{PHL}		30		nS	
Propagation delay time E_2 or E_1 to output	t_{PLH}		19		nS	MV74SC137 and MV74SC237
Propagation delay time E_2 or E_1 to output	t_{PHL}		29		nS	
Propagation delay time E to output	t_{PLH}		19		nS	MV74SC138 and MV74SC238
Propagation delay time E to output	t_{PHL}		29		nS	
Propagation delay time E to output	t_{PLH}		17		nS	MV74SC139 and MV74SC239
Propagation delay time E to output	t_{PHL}		27		nS	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}	3.0	5	7.0	V
High level output current	I_{OH}		−24		mA
Low level output current	I_{OL}		24		mA
Operating free-air temperature	T_A	0		70	°C

3. Voltages are with respect to V_{SS}/GND

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	−0.5V to 7.0V
Input voltage	V_I	−0.3V to V_{CC} + 0.3V
Output current, each output	I_O	± 75mA
Operating temperature	T_A	−40°C to +85°C
Storage temperature	T_S	−65°C to 150°C
Package power dissipation	P	450mW

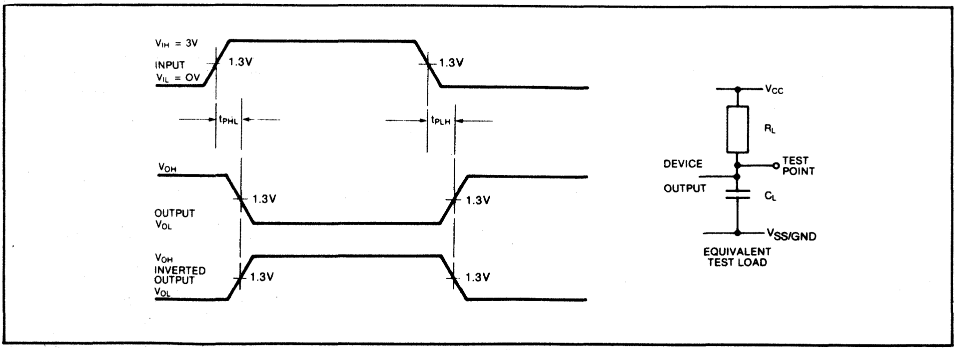


Fig.7 Propagation Delay Times

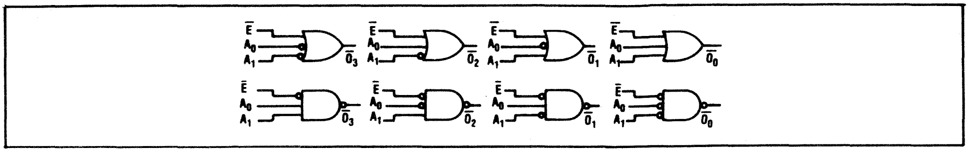


Fig.8 Logic Reduction Application: 4 minterms of 2 variables by MV74SC139

PIN FUNCTIONS

PIN	DESCRIPTION
A_0, A_1, A_2 or A_{0a}, A_{0b} A_{1a}, A_{1b}	Select (Address) Inputs, to be decoded
$\overline{E}_1$, $\overline{E}_2$, E_3 or $\overline{E}_a$, $\overline{E}_b$ or $\overline{E}_1$, E_2	Chip Enable Inputs
LE	Latch Enable Input
O_0 - O_7 or $\overline{O}_0$ - $\overline{O}_7$	Decoded Outputs Inverted Decoded Outputs
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

PLESSEY Semiconductors **ADVANCE INFORMATION** CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV74SC240, MV74SC241, MV74SC244 MV74SC540, MV74SC541

THREE-STATE OCTAL BUFFERS/LINE DRIVERS

This family of ISO-CMOS Octal Buffers and Line Drivers is designed to improve PC board density and performance in three-state memory address drivers, clock drivers and bus oriented receivers and transmitters. A comprehensive range of devices covers a selection of differing input/output pin layouts, inverting and non-inverting buffers and a choice of similar or complementary output controls (E_A, E_B).

The devices are available in the 20-pin DIL (DG) package.

FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- Bus Oriented 3-state outputs
- High Current Sink/Source Capability

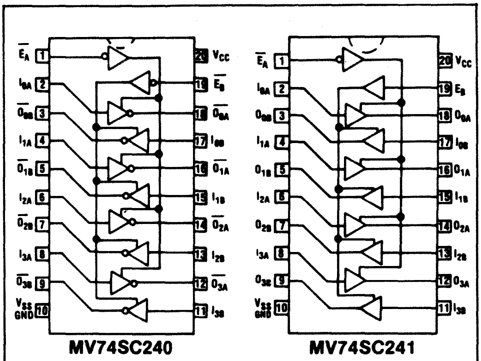
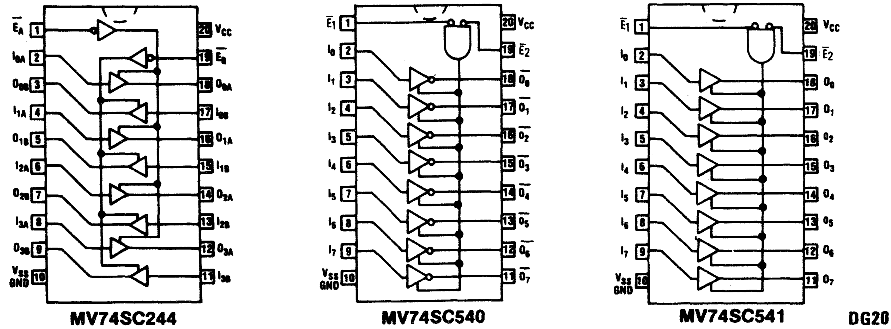


Fig.1 Pin connections (top view)



TRUTH TABLES

INPUTS		OUTPUT	
$\bar{E}$	I_{0-3}	MV74SC240 $\bar{O}_{0-3}$	MV74SC244 O_{0-3}
L	L	H	L
L	H	L	H
H	X	Z	Z

A or B Buffers

MV74SC241					
A BUFFERS			B BUFFERS		
INPUTS		OUTPUT	INPUTS		OUTPUT
$\bar{E}_A$	I_{0-3}	O_{0-3}	E_B	I_{0-3}	O_{0-3}
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

INPUTS			OUTPUT	
$\bar{E}_1$	$\bar{E}_2$	I_{0-7}	MV74SC540 O_{0-7}	MV74SC541 O_{0-7}
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

L Logic Low
H Logic High
X Don't Care
Z High Impedance

DEVICE SELECTION

PRODUCT	3-STATE CONTROL	DATA OUTPUTS
MV74SC240	$\bar{E}_A$, $\bar{E}_B$	inverting
MV74SC241	$\bar{E}_A$, E_B	non-inverting
MV74SC244	$\bar{E}_A$, $\bar{E}_B$	non-inverting
MV74SC540	$\bar{E}_1$ AND $\bar{E}_2$	inverting
MV74SC541	$\bar{E}_1$ AND $\bar{E}_2$	non-inverting

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	− 0.5V to 7.0V
Input voltage	V_I	− 0.3V to Vcc + 0.3V
Output current, per output	I_O	± 75mA
Operating temperature	T_A	− 40 °C to + 85 °C
Storage temperature	T_S	− 65 °C to 150 °C
Package Power dissipation	P	450mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}	3	5	7	V
High level output current	I_{OH}		− 24		mA
Low level output current	I_{OL}		24		mA
Operating free-air temperature	T_{amb}	0		70	°C

1. Voltage values are with respect to V_{SS}/GND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 0°C$ to $+70°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	
Hysteresis (V_T+ − V_T-)	V_O	0.2	0.5		V	
High level output voltage	V_{OH}	2.4 4.35			V V	V_{CC} = 4.75V, I_{OH} = − 14mA I_{OH} = − 3mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 12mA
Off-state output current, high-level voltage applied	I_{OZH}			20	µA	V_{CC} = 5.25V, V_O = 2.7V
Off-state output current, low-level voltage applied	I_{OZL}			− 20	µA	V_{CC} = 5.25V, V_O = 0.4V
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			− 10	µA	V_{CC} = 5.25V, V_I = 0.4V
Short circuit output current	I_{OS}		− 40		mA	NOTE 2 V_{CC} = 5.25V
Supply current	I_{CC}		1	0.1	mA	V_{CC} = 5.25V, outputs disabled

2. Max. dissipation or 1mS duration should not be exceeded.
3. All Typical values at T_A = 25 °C V_{CC} = 5V

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{CC} = 5V$, $T_{amb} = +25°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Propagation delay time, low-to-high-level output	t_{PLH}		12		nS	C_L = 45pF, R_L = 667
Propagation delay time, high-to-low-level output	t_{PHL}		15		nS	
Output enable time to low level	t_{PZL}		20		nS	C_L = 5pF, R_L = 667
Output enable time to high level	t_{PZH}		15		nS	
Output disable time from low level	t_{PLZ}		20		nS	
Output disable time from high level	t_{PHZ}		10		nS	

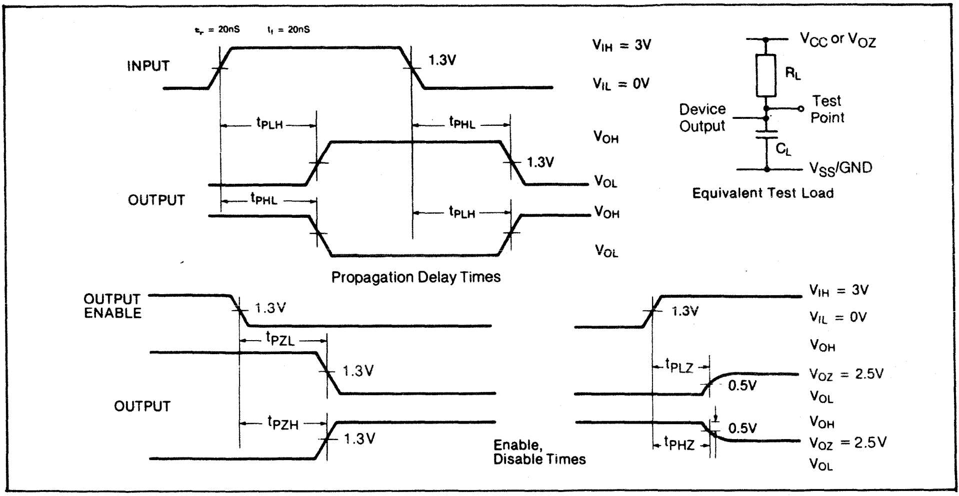


Fig.2 Voltage waveforms

PIN FUNCTIONS

PIN	DESCRIPTION
$\overline{E}_A$, $\overline{E}_B$ $\overline{E}_1$, $\overline{E}_2$ $\overline{E}_A$, E_B	Data Output Enable
I_{0A} - I_{3A} I_{0B} - I_{3B} or I_{0-7}	Data Inputs
O_{0A} - O_{3A} O_{0B} - O_{3B} or O_0 - O_7	Data Outputs
$\overline{O}_{0A}$ - $\overline{O}_{3A}$ $\overline{O}_{0B}$ - $\overline{O}_{3B}$ or $\overline{O}_0$ - $\overline{O}_7$	Inverted Data Outputs
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

PLESSEY
Semiconductors

ADVANCE INFORMATION CMOS

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MV74SC245 MV74SC545

OCTAL BUS TRANSCEIVERS WITH 3-STATE BUFFERED OUTPUTS

These octal bus transceiver circuits are designed for high-speed asynchronous two-way communication between data buses. The control function inputs minimize external timing requirements.

The devices provide data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control input (DIR) pin. The enable input ($\overline{E}$) pin can be used to disable the device outputs so that the buses are effectively isolated from each other. The MV74SC545 differs from the MV74SC245 by use of inverting buffers.

The devices are available in 20-pin DIL(DG)package.

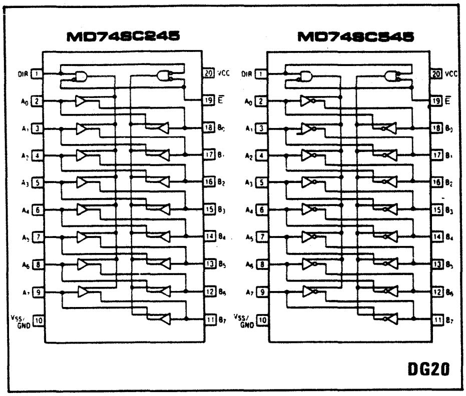

Fig.1 Pin connections and logic diagrams (top view)

FEATURES

- Pin Compatible with 74LS245 Types
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Bus Oriented 3-state Outputs
- Improved Noise Margins, with Input Hysteresis
- High Performance Input/Output Clamping
- Fully TTL compatible, Inputs and Outputs

PIN FUNCTION

Pin	Description
A_0 - A_7	Bus A, Data Inputs/Outputs
B_0 - B_7	Bus B, Data Inputs/Outputs
DIR	Direction Control Input
$\overline{E}$	Enable Input, Active LOW
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

FUNCTION TABLE

Enable $\overline{E}$	Direction Control DIR	Operation
L	L	B → A
L	H	A → B
H	X	Isolation

H = High Level, L = Low Level, X = Don't Care

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
High Level Input Voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis (V_T+ − V_T-)			0.3		V	
High Level Output Voltage	V_{OH}	2.4 4.0			V V	V_{CC} = 4.75V I_{OH} = −14mA I_{OH} = −3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V I_{OL} = 7mA
Offstate Output Current, High Level Voltage Applied	I_{OZH}			20	µA	V_{CC} = 5.25V V_O = 2.7V
Offstate Output Current, Low Level Voltage Applied	I_{OZL}			−20	µA	V_{CC} = 5.25V V_O = 0.4V
Input Current at Maximum Input Voltage	I_I			15	µA	V_{CC} = 5.25V V_I = 5.55V
High Level Input Current (Note 1)	I_{IH}			10	µA	V_{CC} = 5.25V V_{IH} = 2.7V
Low Level Input Current(1)	I_{IL}			−10	µA	V_{CC} = 5.25V V_{IL} = 0.4V
Short Circuit Output Current	I_{OS}		−40		mA	V_{CC} = MAX (Note 2)
Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V Outputs disabled

Note 1. Inputs DIR and $\overline{E}$
Note 2. Max. dissipation or 1 ms should not be exceeded
Note 3. All Typ. values at T_A = 25°C, V_{CC} = 5V

SWITCHING CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = 5V T_{amb} = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Propagation Delay Time Low to High Output	t_{PLH}		22		nS	C_L = 45pF R_L = 667Ω
Propagation Delay Time High to Low Input	t_{PHL}		25		nS	
Output Enable Time to Low Level	t_{PZL}		41		nS	
Output Enable Time to High Level	t_{PZH}		40		nS	
Output Disable Time from Low Level	t_{PLZ}		32		nS	C_L = 5pF R_L = 667Ω
Output Disable Time from High Level	t_{PHZ}		40		nS	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Value
Supply Voltage	V_{CC}	−0.5V to 7.0V
Input Voltage	V_I	−0.3V to V_{CC} + 0.3V
Output Current	I_O	±75mA
Storage Temperature	T_S	−65°C to 150°C
Operating Temperature	T_{amb}	−40°C to 85°C
Power Dissipation	P	450mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3	5	7	V
High Level, Output Current	I_{OH}		−24		mA
Low Level, Output Current	I_{OL}		24		mA
Operating Temperature	T_{amb}	0		70	°C

Note: 4. Voltages are with respect to V_{SS}/GND

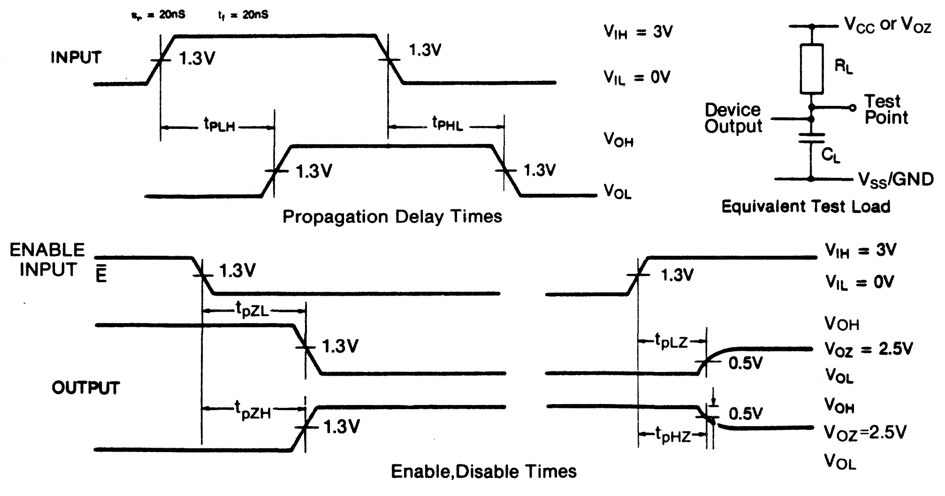

Fig.2 Voltage waveforms

PLESSEY Semiconductors **ADVANCE INFORMATION** **CMOS**

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MV74SC373, MV74SC374, MV74SC533 MV74SC534, MV74SC563, MV74SC564 MV74SC573, MV74SC574

3-STATE OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE TRIGGERED FLIP-FLOPS

This family of 8 bit latches features 3-state operation and is designed for use in high speed, bus oriented systems. The '373 appears transparent to data (outputs change asynchronously) when Latch Enable, $\overline{LE}$, is HIGH. When $\overline{LE}$ is LOW, data meeting the set up times becomes latched. The '374 latches hold their individual data when meeting set up times with the clock, CK, LOW-to-HIGH transition. With both devices $\overline{OE}$ does not affect the state of the latches, but when $\overline{OE}$ is HIGH the outputs become high impedance. Data may thus be latched even when the device is deselected. The family offers a choice of inverted or non-inverted outputs.

The devices are available in 20-lead ceramic DIL (DG) package.

FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- Bus Oriented 3-State Outputs
- High Current, Sink/Source Capability

DEVICE SELECTION

Product	Format	Output
MV74SC373	transparent latch	non-inverted
MV74SC374	D type flip-flop	non-inverted
MV74SC533	transparent latch	inverted
MV74SC534	D type flip-flop	inverted
MV74SC563	transparent latch	inverted
MV74SC564	D type flip-flop	inverted
MV74SC573	transparent latch	non-inverted
MV74SC574	D type flip-flop	non-inverted

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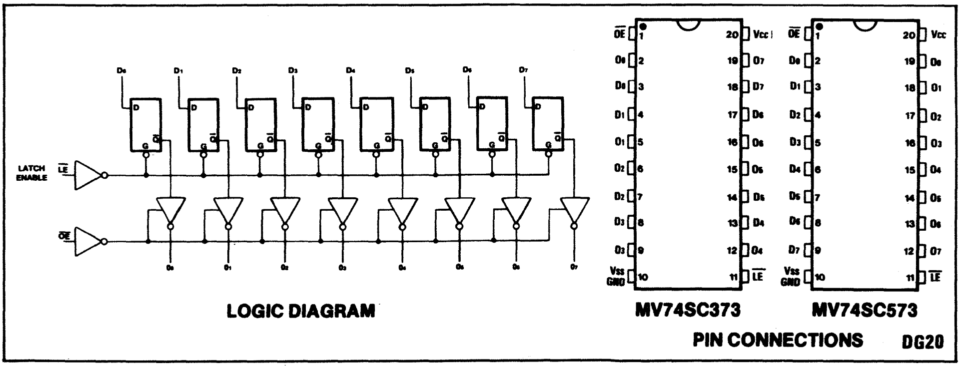


Fig.1 MV74SC373 and MV74SC573

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{CC}	3	5	7	V
High level output current		I_{OH}		−24		mA
Low level output current		I_{OL}		24		mA
Operating free-air temperature		Tamb	0		70	°C
Width of clock/enable pulse,		t_w	15			nS
Data set up time	MV74SCXX3 MV74SCXX4	t_{su}	0↓	2↓ 20↑		nS nS
Data hold time	MV74SCXX4 MV74SCXX4	t_h	10↓ 0↑			nS nS

1. The arrow indicates clock/enable transition: ↑LOW to HIGH, ↓HIGH to LOW
2. Voltage values are with respect to V_{SS}/GND

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 0°C$ to $+70°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis (V_T+ − V_T−) $\overline{LE}$,CK,$\overline{OE}$			0.3		V	
High level output voltage	V_{OH}	2.4 4.35			V V	V_{CC} = 4.75V, I_{OH} = -10mA I_{OH} = -2mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current any input	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			−10	µA	V_{CC} = 5.25V, V_I = 0.4V
Off-state output current high-level voltage applied	I_{OZH}			20	µA	V_{CC} = 5.25V, V_O = 2.7V
Off-state output current,low-level voltage applied	I_{OZL}			−20	µA	V_{CC} = 5.25V, V_O = 0.4V
Short circuit current (Note 3)	I_{OS}		−40		mA	V_{CC} = 5.25V
Quiescent supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs disabled

3. Max. dissipation or 1mS duration should not be exceeded.
4. All TYP. values at Tamb = 25°C V CC = 5V

SWITCHING CHARACTERISTICS (Fig. 5)

Test conditions (unless otherwise stated):
$V_{CC} = 5V$, $T_{amb} = +25°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Propagation delay time, low-to-high level output	t_{PLH}		55 60		nS	MV74SC373, MV74SC573 MV74SC533, MV74SC563 MV74SC374, MV74SC574 MV74SC534, MV74SC564 C_L = 45pF R_L = 667
Propagation delay time high-to-low level output	t_{PHL}		55 60		nS	
Output enable time to low level	t_{PZL}		40		nS	C_L =5 pF R_L = 667
Output enable time to high level	t_{PZH}		40		nS	
Output disable time from low level	t_{PLZ}		33		nS	
Output disable time from high level	t_{PHZ}		72		nS	
Operating frequency	f_{MAX}		20		MHZ	Note 5

5. Maximum clock frequency is tested with all outputs loaded.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	−0.5V to 7.0V
Input voltage	V_I	−0.3V to V_{CC} + 0.3V
Output current, per output	I_O	± 75mA
Operating temperature	Tamb	−40°C to +85°C
Storage temperature	T_S	−65°C to 150°C
Package power dissipation	P	450mW

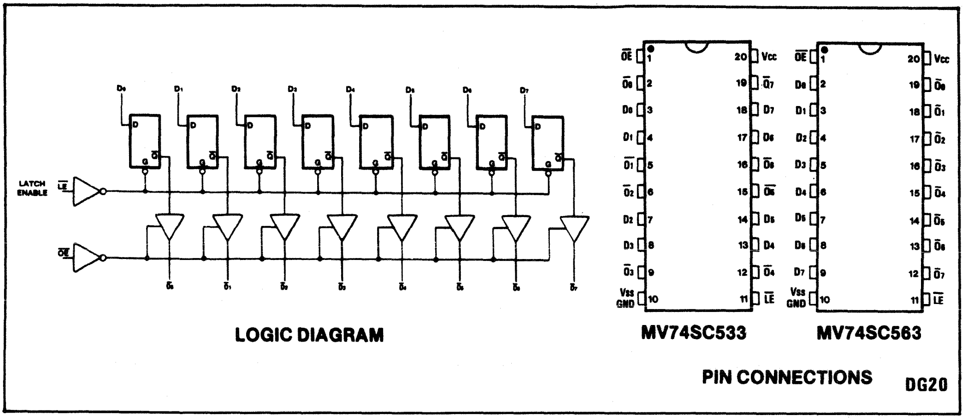


Fig.2 MV74SC533 and MV74SC563

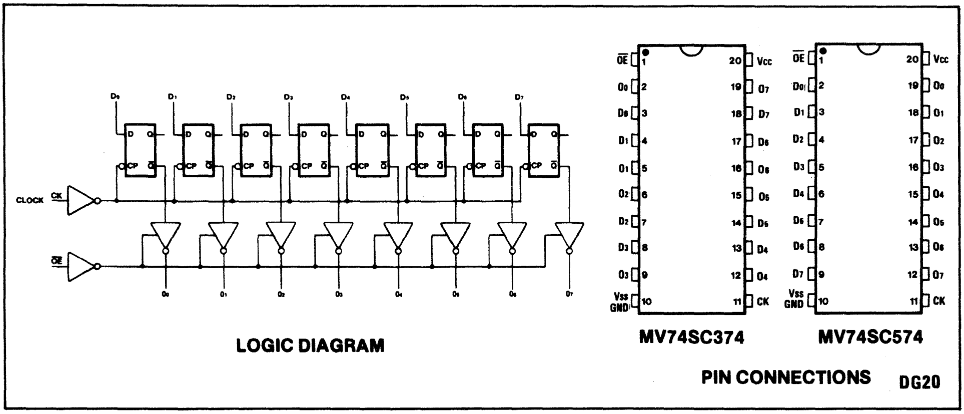


Fig.3 MV74SC374 and MV74SC574

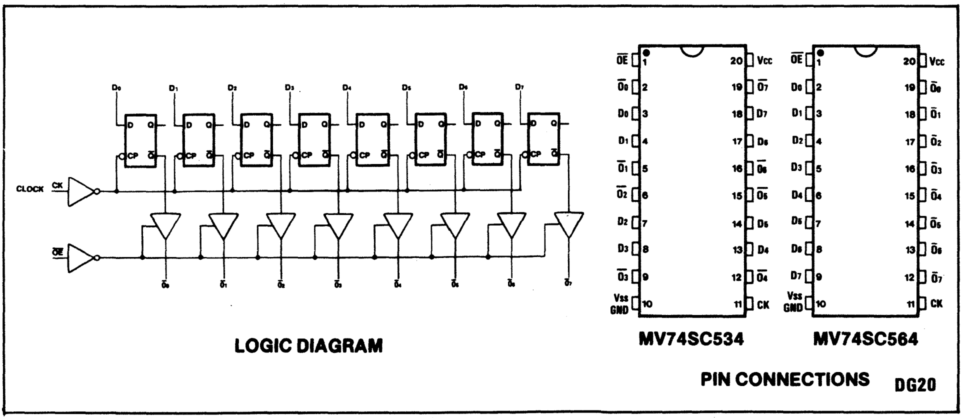


Fig.4 MV74SC534 and MV74SC564

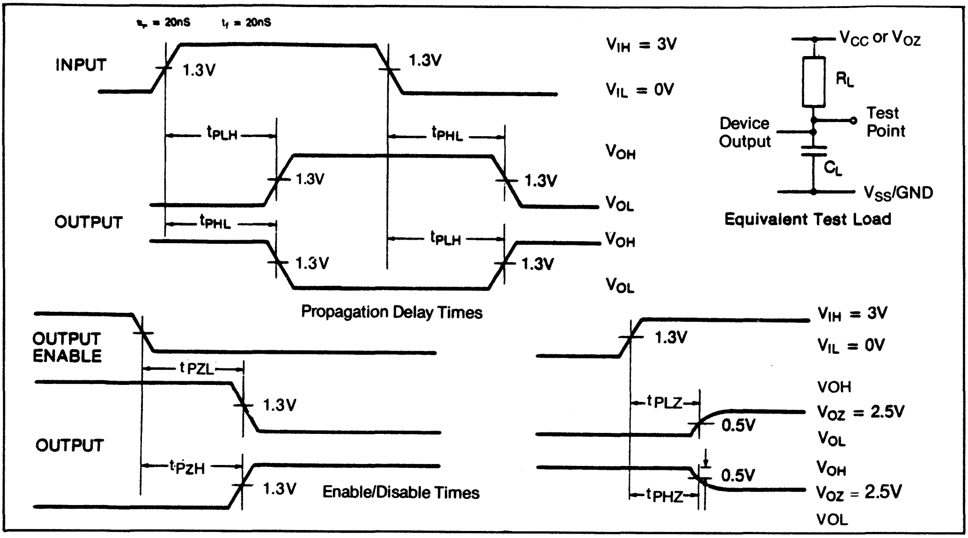


Fig.5 Voltage waveforms (enable, disable and propagation delay times)

PIN FUNCTIONS

Pin	Description
D_{0-7}	Data Inputs
O_{0-7}	Non Inverted Data Outputs
$\overline{O}_{0-7}$	Inverted Data Outputs
$\overline{OE}$	Output Enable
CK	Clock Input
$\overline{LE}$	Latch Enable
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

PLESSEY Semiconductors **ADVANCE INFORMATION CMOS**

MV8820

DUAL-TONE MULTI-FREQUENCY (DTMF) RECEIVER/DECODER

The MV8820 is a CMOS/LSI circuit designed to detect all 16 DTMF combinations of mixed tones using digital circuit techniques. The circuit accepts the tones after filtering, separating and squaring of the high and low frequency groups. It then converts the input signals into digital output codes which represent the number that was originated at the transmitting unit. The circuit will accurately discriminate between adjacent frequencies in both the high and low bands in the presence of noise and normal voices. The actual algorithm used was developed empirically in actual telecommunication environments and by using the statistical differences between noise, tone and speech.

The internal timebase uses a 3.58MHz crystal to provide accurate detection. A built-in Power-On Reset ensures proper start-up whenever power is applied or reapplied to the circuit. Either 5V or 12 to 15V operation is offered as a result of an on-chip power supply regulator circuit.

The output code converter consists of a ROM which provides two different 8-bit code formats. These are; a 2-of-8 (4 rows and 4 columns) or 4-bit hexadecimal and a 4-bit code compatible with the GIAY-5-9100 Dial Pulse Converter circuit. The 8 outputs are latched and buffered 3-state circuitry.

FEATURES

- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times Down to 20ms
- 5V to 15V Operation
- Latched 3-State Buffered Outputs
- STD 24 Pin Package
- Detects all 16 DTMF Combinations
- 3 Output Codes Available
- Uses STD 3.58MHz TV Crystal
- Built-In Power-On Reset
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times

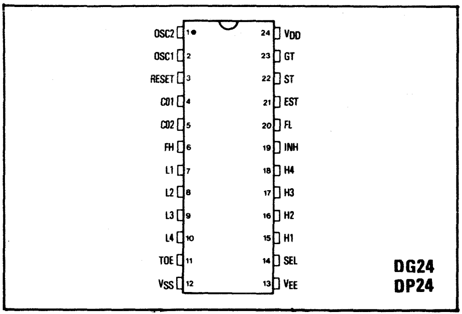


Fig.1 Pin connections

Steering logic and a guard time input are provided to offer adjustable 'acquire time' and 'release time' of circuit. The MV8820 is available in Plastic DIL (DP, -40°C to C+85°C), Ceramic DIL (DG, -40°C to +85°C).

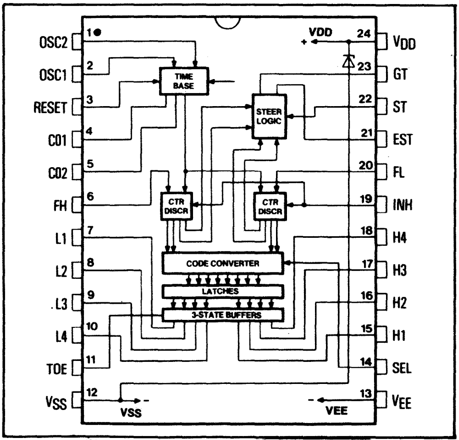
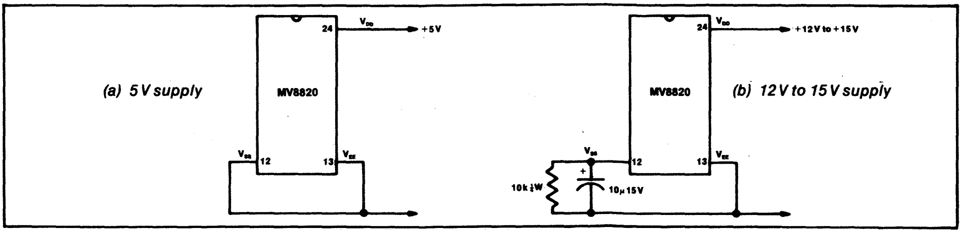


Fig.2 MV8820 functional block diagram



(a) 5V supply

(b) 12V to 15V supply

Fig.3 Power supply optional connections

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1 2	OSC 2 OSC 1	**Oscillator Inputs.** Input and output of inverter circuit, to which a 3.57954S MHz TV color-burst crystal is connected.
3	RESET	**Reset Input.** A logic HIGH on this pin causes the circuit to be reset to start of detect mode.
4 5	CO 1 CO 2	**18.2KHz Clock Outputs.** Non-overlapping active-level HIGH signals for use with external circuits.
6	FH	**High Frequency Group (active HIGH) Input.** Accepts and detects the high band frequencies of 1209Hz, 1336Hz, 1477Hz and 1633Hz.
7 8 9 10	L 1 L 2 L 3 L 4	**Low-Group (active HIGH) Outputs.** With a logic HIGH on the SEL Input (pin 14), this low-group output will provide the low end of the 2-of-8 code format when combined with the high-group outputs. A logic LOW on SEL (pin 14) will cause these to provide a hexadecimal code format output.
11	TOE	**3-State Output Enable Input.** A logic HIGH on this input pin will cause the 8 buffered outputs to remain in their high-impedance state.
12	VSS	Negative Logic Voltage Input Terminal.
13	VEE	Negative Voltage Input Terminal.
14	SEL	**Select Code Input.** A logic HIGH on this input selects the 2-of-8 code output on L1, L2, L3, L4, H1, H2, H3, H4 pins. While a logic LOW on this pin causes L1, L2, L3, L4 to be a hexadecimal code, and H1, H2, H3, H4 to be in a code format compatable for the G.I. AY-5-9100 device.
15 16 17 18	H1 H2 H3 H4	**High-Group (active HIGH) outputs.** A logic HIGH on the SEL input (pin 14) cause these outputs to provide the high end of a 2-of-8 code format when combined with the low-group outputs. When a logic LOW is applied to the SEL input, these outputs provide a code which is compatable with the GI AY-5-9100 device.
19	INH	**Inhibit Input.** A logic HIGH on this input pin will inhibit the circuit from detecting the input frequencies corresponding to the 6 tone-pairs normally not used. This further improves "talk-off" for these applications.
20	FL	**Low Frequency Group (active HIGH) Input.** Accepts and detects the low band frequencies of 697Hz, 770Hz, 852Hz and 941Hz.
21	EST	**Early Steering (active HIGH) Output.** This output will go to a logic HIGH state as soon as a recognizable tone-pair is detected. A noise spike, a frequency drift or even a monentary drop in the incoming tones will cause this pin to return to a logic LOW state.
22	ST	**Steering Input.** A logic HIGH level applied to this input will cause the circuit to accept and latch the code for the tone-pair detected. It also causes the GT output (pin 21) to go to a logic HIGH. A logic LOW level on this pin will release the circuit to accept a new tone-pair. GT output will return to a logic LOW state.
23	GT	**Guard Time Output.** This output goes to a logic HIGH when the circuit detects and accepts a valid tone-pair. It will return to a logic LOW whenever the ST input (pin22) detects logic LOW level.
24	VDD	Positive Voltage Input Terminal

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

MV8820

DC Supply Voltage, V_{DD}	-0.5 to +16V
Logic Negative Supply, V_{SS}	-0.5V to V_{DD}
Input Voltage, All Inputs, V_{IN}	-0.25 to V_{DD} +0.25V
Operating Temperature Range, T_{amb}	-40°C to +85°C
Storage Temperature Range, T_{STG}	DG: -55°C to +175°C DP: -55°C to +125°C

OUTPUT FORMATS		SEL=H (2-of-8 Code)									SEL = L (Hexadecimal Code), H format compatible with GIAV-5-9100 Unit.							
		L1	L2	L3	L4	H1	H2	H3	H4		L1	L2	L3	L4	H1	H2	H3	H4
ORIGINAL DATA TRANSMITTED	1	H	L	L	L	H	L	L	L		H	L	L	L	L	L	L	L
	2	H	L	L	L	L	H	L	L		L	H	L	L	L	H	L	L
	3	H	L	L	L	L	L	H	L		H	H	L	L	L	L	H	L
	4	L	H	L	L	H	L	L	L		L	L	H	L	L	L	L	H
	5	L	H	L	L	L	H	L	L		H	L	H	L	L	H	L	H
	6	L	H	L	L	L	L	H	L		L	H	H	L	L	L	H	H
	7	L	L	H	L	H	L	L	L		H	H	H	L	H	L	L	L
	8	L	L	H	L	L	H	L	L		L	L	L	H	H	H	L	L
	9	L	L	H	L	L	L	H	L		H	L	L	H	H	L	H	L
	0	L	L	L	H	L	H	L	L		L	H	L	H	L	H	H	L
	*	L	L	L	H	H	L	L	L		H	H	L	H	H	L	H	H
	✱	L	L	L	H	L	L	H	L		L	L	H	H	H	L	L	H
	A	H	L	L	L	L	L	L	H		H	L	H	H	H	H	H	L
	B	L	H	L	L	L	L	L	H		L	H	H	H	H	H	L	H
	C	L	L	H	L	L	L	L	H		H	H	H	H	L	H	H	H
	D	L	L	L	H	L	L	L	H		L	L	L	L	H	H	H	H

Table 1 Output truth table

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ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV8860

DTMF DECODER

The MV8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (MV8865) and provides a 3-state buffered 4-bit binary output. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8860 is implemented in CMOS technology and incorporates an on-chip regulator, providing low power operation and power supply flexibility.

The MV8860 is available in Plastic DIL (DP) and Ceramic DIL (DG), both with an operating temperature range of -40°C to +85°C.

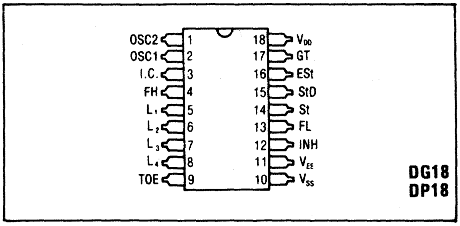


Fig.1 Pin connections (top view)

FEATURES

- 18 Pin DIL Package
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5 V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

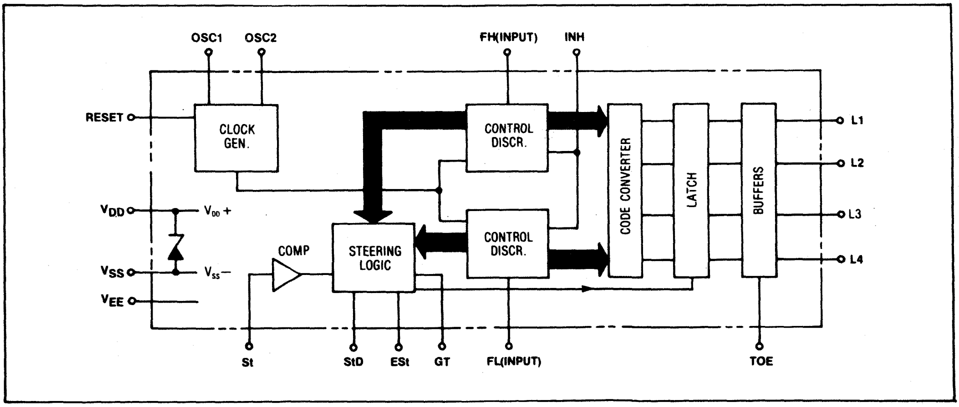


Fig.2 MV8860 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$; $f_c = 3.579545MHz$
5 V operation: $V_{DD} - V_{EE} = 5V$, $V_{SS} = V_{EE}$, connections as Fig.5a
12 V operation: $V_{DD} - V_{EE} = 12V$, $R_{SSEE} =$ 2.5k, connections as Fig.5b
Outputs not loaded
For input current parameters only, $V_{IH} = V_{IHO} = V_{DD}$, $V_{IL} = V_{EE}$, $V_{ILO} = V_{SS}$
All voltages referenced to V_{EE} unless otherwise noted.

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		15	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4						6.5		V	Connections Fig. 5b
5		Operating Supply Current		I_{DD}		1.3		mA	5V
6						2.5		mA	12V
7		Internal Logic Ground Pin Current		I_{SS}		−2.2		mA	12V
8		Operating Power Consumption		P_O		6.5		mW	5V
9						30		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}		4		V	5V
11						9		V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}		1		V	5V
13						3		V	12V
14		High Level Input Voltage OSC1		V_{IHO}		4.5		V	5V
15						11		V	12V
16		Low Level Input Voltage OSC1		V_{ILO}		0.5		V	5V Ref V_{SS}
17						0.5		V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSt}		2.5		V	5V
19						6		V	12V
20		Pull Down Sink Current (INH)		I_{IHI}		25		μA	5V
21						190		μA	12V
22		Pull Up Source Current (TOE)		I_{ILT}		7		μA	5V
23						55		μA	12V
24		Input High Leakage Current		I_{IH}		1		μA	5V or 12V
25		Input Low Leakage Current		I_{IL}		1		μA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}		4.5		V	5V
27						11		V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}		0.5		V	5V
29						1		V	12V
30		High Level Output Voltage OSC2		V_{OHO}		4.5		V	5V
31						11.5		V	12V
32	OUTPUTS	Low Level Output Voltage OSC2		V_{OLO}		0.5		V	5V Ref V_{SS}
33						0.5		V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}		0.5		mA	5V V_{OH} = 4.5V
35						0.5		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}		1.0		mA	5V V_{OL} = 0.5V
37						1.0		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OHO}		100		μA	5V V_{OH} = 4.5V
39						100		μA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OLO}		150		μA	5V V_{OL} = 0.5V
41						150		μA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	$L_1 - L_4$ = H	I_{OZ}		35		nA	5V Appl V_{OL} = 0V
43			$L_1 - L_4$ = L			100		nA	5V Appl V_{OH} = 5V
44			$L_1 - L_4$ = H			100		nA	12V Appl V_{OL} = 0V
45			$L_1 - L_4$ = L			300		nA	12V Appl V_{OH} = 12V

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{DD} = +5V; f_c = 3.579545MHz

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A		±2.5		% Nom.		
2		Tone Frequency Deviation Reject		Δf_R		±3.5		% Nom.		
3		Tone Present Detection Time		t_{DP}	8	10	15	ms		
4		Tone Absent Detection Time		t_{DA}	0.6	4	10	ms		
5		Guard Time (Adjustable)		$t_{GT(P\ or\ E)}$		20		ms	See Fig. 3 Fig. 7a R = 300k Ω C = 0.1μF	
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}	28	30	35	ms		
7		Invalid Tone Duration (f_n of $t_{\overline{REC}}$)		$t_{\overline{REC}}$			20	ms		
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}	30			ms		
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}			20	ms		
10	I/P	FL FH Input Transition Time		t_T				us	10% - 90% V_{DD}	
11		Capacitance Any Input		C		5		pF		
12	OUTPUTS	Propogation Delay St to L_1 - L_4		t_{PL}		8		μs	V_{DD} 5V	
13						8		μs	V_{DD} 12V	
14		Propogation Delay St to StD		t_{PStD}		12		μs	V_{DD} 5V	
15						12		μs	V_{DD} 12V	
16		Propogation Delay TOE to L_1 - L_4	Enable	t_{PTE}		300		ns	V_{DD} 5V	
17						200		ns	V_{DD} 12V	
18			Disable	t_{PTD}		300		ns	V_{DD} 5V	
19						200		ns	V_{DD} 12V	
20	CLOCK	Crystal/Clock Frequency		f_c		3.5795		MHz	OSC 1	OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90%	Externally
22			Fall Time	t_{HLCI}			110	ns	V_{DD} = V_{SS}	Applied
23			Duty Cycle	DC_{CI}		50		%		Clock
24		Clock Output (OSC 2)	Capacitive Load	C_{LOC}				pF	With Clock Drive to OSC 1	
25				C_{LOX}				nF	Sinusoidal Output With Crystal	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	−40	+85	°C
Storage Temperature	DG Package	-55	+175	°C
	DP Package	-55	+125	°C

		Max
Power Dissipation	DG Package*	1000mW
	DP Package**	450mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

~~D3 D2 D1 D0~~

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

(c) Steering

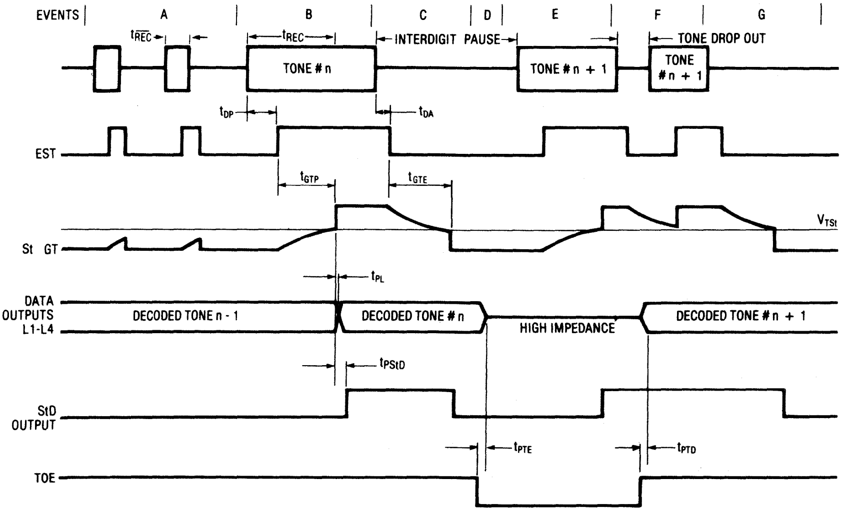
* DELAYED WRT St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H= LOGIC HIGH L= LOGIC LOW
Ø= "DON'T CARE" LOGIC HIGH OR LOW
Z= HIGH IMPEDANCE X= ANY CHARACTER

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter	
5	L1	Data Outputs. 3 state buffered Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE See Table 1 for state table	
6	L2		
7	L3		
8	L4		
9	TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up	
10	V_{SS}	Internal logic ground. For V_{DD} - V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD} - V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 5	
11	V_{EE}	Negative power supply. External logic ground	
12	INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down	
13	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter	
14	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage< V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description	
15	StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}	
16	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low	
17	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
18	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8860 is a CMOS Digital DTMF detector and decoder. Used in conjunction with a suitable DTMF filter (MV8865) it can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8860s FH and FL inputs, respectively. The MV8865 DTMF filter provides these functions.

Within the MV8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When L_1 to L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8860 may be operated from either a 5V or 8 to 15V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8860 with the MV8865 DTMF filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8860 OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

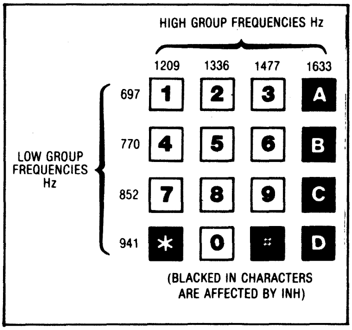


Fig.4 DTMF matrix, indicating character-tone pair correspondence

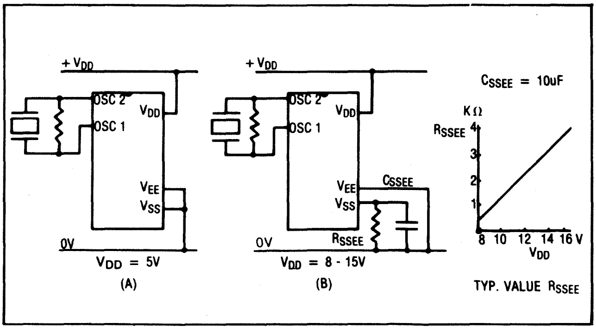
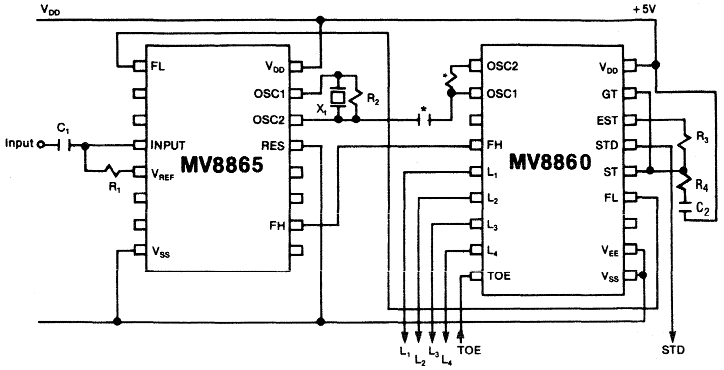


Fig.5 Power supply connection options



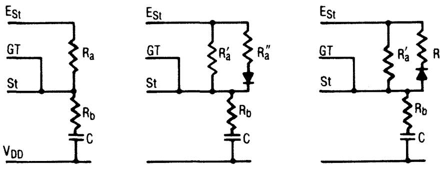
R_1 = 2.0M
R_2 = 2M
R_3 = 300K
R_4 = 5K
C_1 = 10nF
C_2 = 0.1uF
X_t = 3.579MHz

* WITH DEVICE POWER SUPPLY CONNECTED AS FIG. 5B, 33pF CAPACITOR AND 2M RESISTOR REQUIRED

TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	30ms

Fig.6 Single-ended input receiver using the MV8865 (5 V operation)



$T_{GTP} = T_{GTE}$
(A)

$T_{GTP} < T_{GTE}$
(B)

$T_{GTP} > T_{GTE}$
(C)

$$T_{GTP} = C\,(R_a + R_b)\,\mathrm{Logn}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C\,(R_a + R_b)\,\mathrm{Logn}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$
WITH $R_b < 0.1\ R_a$ $\qquad R_b \geqslant V_{DD} - V_{EE}$ KΩ

$$R_b < 0.1 \left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C \left(1 - \frac{R_b}{2\ R_a}\right)$

$$\left.\begin{array}{l}\text{B) } T_{GTP} \\ \text{C) } T_{GTE}\end{array}\right\} \triangleq 0.69\ C \left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

$$\left.\begin{array}{l}\text{B) } T_{GTE} \\ \text{C) } T_{GTP}\end{array}\right\} \triangleq 0.69\ R_a'\ C$$

Fig.7 Guard time adjustment

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ADVANCE INFORMATION CMOS

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MV8862/3

DTMF DECODER

The MV8862 and MV8863 each detect and decode all 16 DTMF tone pairs. The devices accept the high group and low group square wave signals from a DTMF FILTER (MV8865) and provide a 3 state buffered 8 Bit binary output with a choice of 3 coding formats. The two devices differ only in the specific output code formats they provide. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8862/3 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility.

The MV8862/3 are available in Plastic DIL (DP) and Ceramic DIL (DG), both with operating temperature range of -40°C to +85°C.

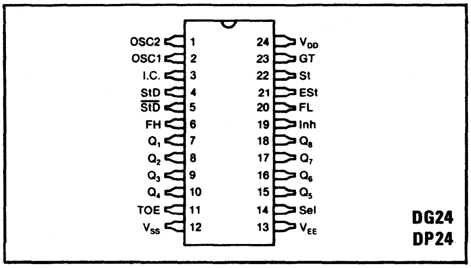


Fig.1 Pin connections (top view)

FEATURES

- Hex or 2 of 8 Output Codes
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5 V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

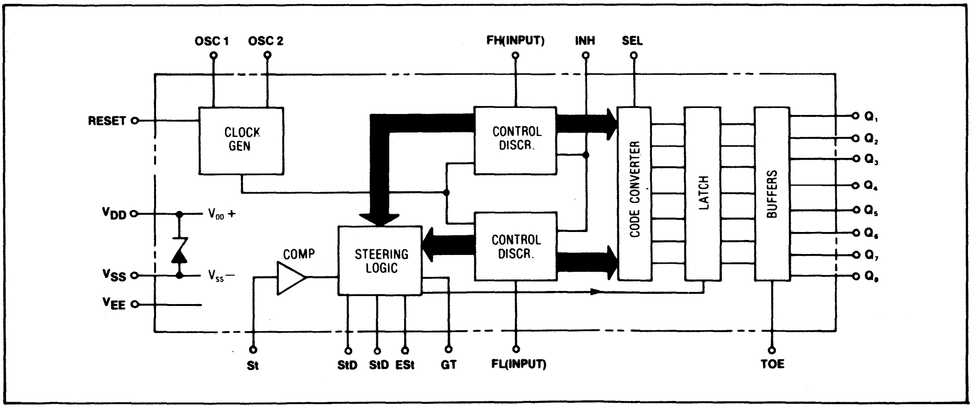


Fig.2 MV8862/3 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = +25°C$; $f_c = 3.579545MHz$
5 V operation: $V_{DD} - V_{EE} = 5V$, $V_{SS} = V_{EE}$, connections as Fig.5a
12 V operation: $V_{DD} - V_{EE} = 12V$, $R_{SSEE} = 900\Omega$, connections as Fig.5b
Outputs not loaded
For input current parameters only, $V_{IH} = V_{IHO} = V_{DD}$, $V_{IL} = V_{EE}$, $V_{ILO} = V_{SS}$
All voltages referenced to V_{EE}

		Characteristics		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4					6.0	6.5	7.5	V	Idd = 7mA
5		Operating Supply Current		I_{DD}		1.3	4	mA	5V
6						2.5	5	mA	12V $V_{DD} - V_{SS} = 5.5V$
7		Internal Logic Ground Pin Current		I_{SS}		5.52	6.7	mA	12V $R_{SSEE} = 900\Omega$
8		Operating Power Consumption		P_o		6.5		mW	5V
9						66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}	3.5			V	5V
11					8.5			V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}			1.5	V	5V
13							3.5	V	12V
14		High Level Input Voltage OSC1		V_{IHO}	3.5			V	5V
15					10.5			V	12V
16		Low Level Input Voltage OSC1		V_{ILO}			1.5	V	5V Ref V_{SS}
17							1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSt}	2.04	2.27	2.5	V	5V
19					5.4	6.00	6.6	V	12V
20		Pull Down Sink Current (INH, Sel)		I_{SI}	10	25	75	µA	5V
21					10	190	400	µA	12V
22		Pull Up Source Current (TOE)		I_{SO}	2	7	45	µA	5V
23					2	7	45	µA	12V
24		Input High Leakage Current		I_{IH}		0.1	1.5	µA	5V or 12V
25		Input Low Leakage Current		I_{IL}		0.1	1.5	µA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}	4.9			V	5V
27					11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}			0.1	V	5V
29							0.1	V	12V
30		High Level Output Voltage OSC2		V_{OH}	4.9			V	5V
31					11.9			V	12V
32	OUTPUTS	Low Level Output Voltage OSC2		V_{OL}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V $V_{OH} = 4.6V$
35					0.5	0.8		mA	12V $V_{OH} = 11.5V$
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V $V_{OL} = 0.4V$
37					1.0	1.6		mA	12V $V_{OL} = 0.5V$
38		Output Drive Current OSC2	P Channel Source	I_{OH}	90	120		µA	5V $V_{OH} = 4.6V$
39					90	120		µA	12V $V_{OH} = 11.5V$
40			N Channel Sink	I_{OL}	100	160		µA	5V $V_{OL} = 0.4V$
41					100	160		µA	12V $V_{SS} = 0.5V$
42		Tristate Output Current (High Impedance State)	$Q_1 - Q_8 = H$	I_{OZ}		0.035	1.5	µA	5V Appl $V_{OL} = 0V$
43			$Q_1 - Q_8 = L$			0.10	1.5	µA	5V Appl $V_{OH} = 5V$
44			$Q_1 - Q_8 = H$			0.10	1.5	µA	12V Appl $V_{OL} = 0V$
45			$Q_1 - Q_8 = L$			0.30	1.5	µA	12V Appl $V_{OH} = 12V$

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$; $V_{DD} = +5V$; $f_c = 3.579545MHz$

		Characteristic		Symbol	Min	Typ*	Max	Unit	Test Conditions	
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.		
2		Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.		
3		Tone Present Detection Time		t_{DP}	8	10	15	ms		
4		Tone Absent Detection Time		t_{DA}	0.6	4	10	ms		
5		Guard Time		$t_{GT(P\ or\ E)}$	Adjustable. Functions of t_{GT}. See Figs 3, 6, 7.					
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}						
7		Invalid Tone Duration (f_n of t_{REC})		$t_{\overline{REC}}$						
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}						
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}						
10	I/P	FL FH Input Transition Time		t_T			1.0	µs	10% - 90% V_{DD}	
11		Capacitance Any Input		C		5	7.5	pF		
12	OUTPUTS	Delay St to Q_1 - Q_8		t_{PL}		8	11	us	V_{DD} 5V or 12V	
13										
14		Delay St to StD		t_{PStD}		12	14	µs	V_{DD} 5V or 12V	
15		Synch. Delay Q_1 - Q_8 to StD		t_{QStD}		3.43		µs		
16		Propogation Delay TOE to Q_1 - Q_8	Enable	t_{PTE}		300		ns	V_{DD} 5V	
17						200		ns	V_{DD} 12V	
18			Disable	t_{PTD}		300		ns	V_{DD} 5V	
19						200		ns	V_{DD} 12V	
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC 1	OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90% V_{DD} − V_{SS}	Externally Applied Clock
22			Fall Time	t_{HLCI}			110	ns		
23			Duty Cycle	DC_{CI}	40	50	60	%		
24		Clock Output (OSC 2)	Capacitive Load	C_{LO}			30			
25										

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	−40	+85	°C
Storage Temperature	DG Package	-55	+175	°C
	DP Package	-55	+125	°C

		Max
Power Dissipation	DG Package*	1200mW
	DP Package**	600mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Original Tone Character		TOE	Sel	8862								8863							
				Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
	X	L	Ø	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
DR	1	H	L	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L	H
	2	H	L	L	L	H	L	L	L	H	L	L	L	H	L	L	L	H	L
	3	H	L	L	L	H	H	L	L	H	H	L	H	L	L	L	L	H	H
	4	H	L	L	H	L	L	L	H	L	L	H	L	L	L	L	H	L	L
	5	H	L	L	H	L	H	L	H	L	H	H	L	H	L	L	H	L	H
	6	H	L	L	H	H	L	L	H	H	L	H	H	L	L	L	H	H	L
	7	H	L	L	H	H	H	L	H	H	H	L	L	L	H	L	H	H	H
	8	H	L	H	L	L	L	H	L	L	L	L	L	H	H	H	L	L	L
	9	H	L	H	L	L	H	H	L	L	H	L	H	L	H	H	L	L	H
	0	H	L	L	L	L	L	H	L	H	L	L	H	H	L	H	L	H	L
D	*	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	L	H	H
	#	H	L	H	L	H	H	H	H	L	L	H	L	L	H	H	H	L	L
	A	H	L	H	H	L	L	H	H	L	H	L	H	H	H	H	H	L	H
	B	H	L	H	H	L	H	H	H	H	L	H	L	H	H	H	H	H	L
	C	H	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H
	D	H	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
DR	1	H	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L	L	H
	2	H	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L	L	H
	3	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	H
	4	H	H	H	H	H	L	H	H	L	H	L	L	L	H	L	L	H	L
	5	H	H	H	H	L	H	H	H	L	H	L	L	H	L	L	L	H	L
	6	H	H	H	L	H	H	H	H	L	H	L	H	L	L	L	L	H	L
	7	H	H	H	H	H	L	H	L	H	H	L	L	L	H	L	H	L	L
	8	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H	L	L
	9	H	H	H	L	H	H	H	L	H	H	L	H	L	L	L	H	L	L
	0	H	H	H	H	L	H	L	H	H	H	L	L	H	L	H	L	L	L
D	*	H	H	H	H	H	L	L	H	H	H	L	L	L	H	H	L	L	L
	#	H	H	H	L	H	H	L	H	H	H	L	H	L	L	H	L	L	L
	A	H	H	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	H
	B	H	H	L	H	H	H	H	H	L	H	H	L	L	L	L	L	H	L
	C	H	H	L	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L
	D	H	H	L	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*	$\overline{StD}$*
L	L	L	L	H
H	L	Z	L	H
L	H	Z	H	L
H	H	H	H	L

(c) Steering

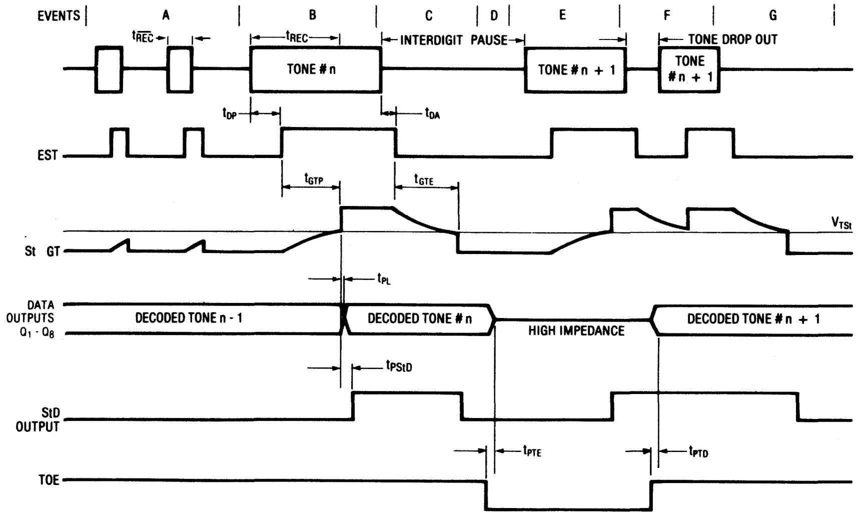
* DELAYED FROM St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H= LOGIC HIGH
X= ANY CHARACTER
L=LOGIC LOW
Z=HIGH IMPEDANCE
Ø="DON'T CARE"
LOGIC HIGH OR LOW

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5M Ω resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	StD	Delayed Steering Output. Flags when a valid tone pair has been received. When the St voltage exceeds V_{TSt}, the output latch is updated, then StD presents a logic high. Returns to logic low when St voltage falls below V_{TSt}. (See Table 1c)	
5	StD	Inverted StD.	
6	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter.	
7	Q1	Data outputs 3 state buffered. Provides 4 bit binary word (Sel. low) or half of 2 of 8 binary word (Sel. high), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.	
8	Q2		
9	Q3		
10	Q4		
11	TOE	3 state output enable input. Logic high on this input enables outputs Q1-Q8. Internal pull up	
12	V_{SS}	Internal logic ground. For $V_{DD} - V_{EE} = 5V$, V_{SS} connected to V_{EE}. For $V_{DD} - V_{EE} > 8V$, V_{SS} connected via resistor to V_{EE} see Fig. 5	
13	V_{EE}	Negative power supply. External logic ground.	
14	Sel.	Output Code Select. Logic low on this pin selects Q1-Q4, Q5-Q8 to provide 2 different 4 bit binary output codes. A logic high selects Q1-Q8 to provide a 2 of 8 output code (See Fig. 2).	
15	Q5	Data outputs 3 state buffered. Provides 4 bit binary word (Sel. low) or half of 2 of 8 binary word (Sel. high), corresponding to the tone pair decoded, when enabled by TOE. See Table 1 for state table.	
16	Q6		
17	Q7		
18	Q8		
19	Inh	Inhibit input. Logic high inhibits detection of tones (D tones in Table 1a) representing characters #, *, A, B, C, D. Internal pull down.	
20	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter.	
21	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low.	
22	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage less than V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description.	
23	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
24	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8862 is a CMOS Digital DTMF Detector and Decoder. The MV8863 is an identical device except that it provides a different set of output codes. The codes of the MV8863 are the same as those provided by MV8820. Used in conjunction with a suitable DTMF filter (MV8865) the MV8862 or MV8863 can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8862(3) must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8862(3)s FH and FL inputs respectively. The MV8865 DTMF Filter provides these functions.

Within the MV8862(3) FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents an 8 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs Q_1 to Q_8. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When Q_1 - Q_8 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8862(3) may be operated from either a 5V or 8 to 13V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8862(3) with the MV8865 DTMF Filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8862(3) OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

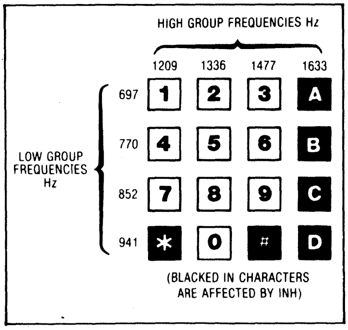


Fig.4 DTMF matrix, indicating character-tone pair correspondence

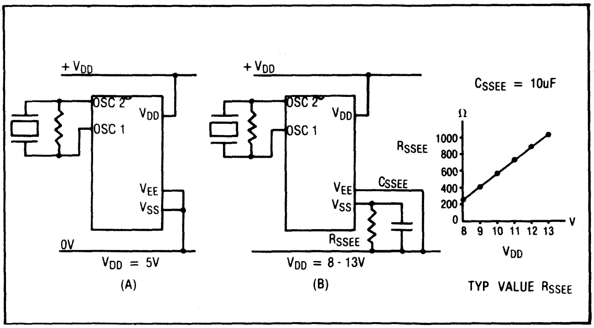
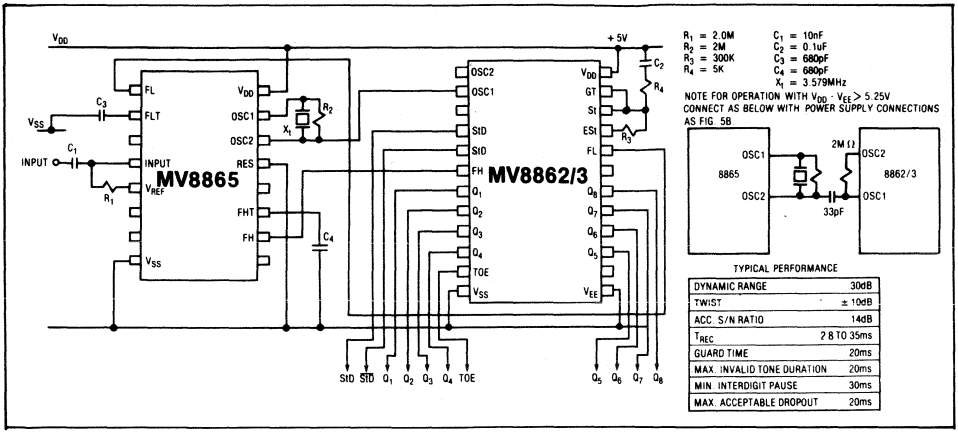


Fig.5 Power supply connection options



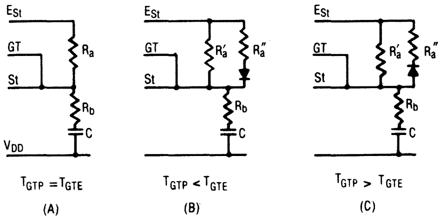
R_1 = 2.0M
R_2 = 2M
R_3 = 300K
R_4 = 5K
C_1 = 10nF
C_2 = 0.1uF
C_3 = 680pF
C_4 = 680pF
X_1 = 3.579MHz

NOTE FOR OPERATION WITH $V_{DD} - V_{EE} > 5.25V$ CONNECT AS BELOW WITH POWER SUPPLY CONNECTIONS AS FIG. 5B.

TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	2 8 TO 35ms
GUARD TIME	20ms
MAX. INVALID TONE DURATION	20ms
MIN. INTERDIGIT PAUSE	30ms
MAX. ACCEPTABLE DROPOUT	20ms

Fig.6 Single-ended input receiver using the MV8865 (5V operation)



$T_{GTP} = T_{GTE}$
(A)

$T_{GTP} < T_{GTE}$
(B)

$T_{GTP} > T_{GTE}$
(C)

$$T_{GTP} = C\,(R_a + R_b)\,\mathrm{LOG}_n\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C\,(R_a + R_b)\,\mathrm{LOG}_n\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{DD}, V_{EE} Symetric About $V_{TSt} = ½\ V_{DD}$
WITH $R_b < 0.1\ R_a$ $\qquad R_b \geqslant V_{DD} - V_{EE}\ K$

$$R_b < 0.1\left(\frac{R_a'\,R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2\,R_a}\right)$

$$\left.\begin{array}{l}\text{B) } T_{GTP}\\ \text{C) } T_{GTE}\end{array}\right\} \triangleq 0.69\ C\left(\frac{R_a'\,R_a''}{R_a' + R_a''}\right)$$

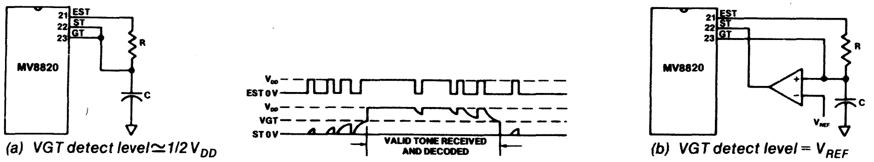
$$\left.\begin{array}{l}\text{B) } T_{GTE}\\ \text{C) } T_{GTP}\end{array}\right\} \triangleq 0.69\ R_a'\ C$$

Fig.7 Guard time adjustment

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

PIN	SYMBOL	CHARACTERISTIC	LIMITS			UNIT	CONDITIONS		
			Min	Typ	Max		VDD	VSS	VEE
24	IDD	Quiescent Current with Osc. operating at 3.58 MHz.		300 1500 2500		μAdc	5V 12V 15V	OV See Fig.3	OV OV OV
–	VIH	Input High Voltage, all inputs.		2.75 9.00		Vdc	VDD = 5V VDD = 15V		
–	VIL	Input LOW Voltage, all inputs.		2.25 6.00		Vdc	VDD = 5V VDD = 15V		
–	VOH	Output HIGH Voltage, all outputs.		4.5 11.5 14.0		Vdc	VDD = 5V, IOH=150μA VDD = 12V, IOH=350μA VDD = 15V, IOH=1.1 μA		
–	VOL	Output LOW Voltage, all outputs.		0.25 0.25 0.25		Vdc	VDD = 5V, IOL=0.4mA VDD = 12V, IOL=0.4mA VDD = 15V, IOL=2.4mA		
–	IOH	Output HIGH Current, all outputs.		−3.0 −3.0 −3.0		μAdc	VDD = 5V, VOH= 2.8V VDD = 12V, VOH= 8.1V VDD = 15V, VOH=13.1V		
–	IOL	Output LOW Current, all outputs.		1.0 3.0 8.0		μAdc	VDD = 5V, VOL=0.4V VDD = 12V, VOL=0.5V VDD = 15V, VOL=1.5V		
6/20	STV STV IPT IDT	Signal Time Valid Signal Time Not Valid Interdigit Pause Time Interdigit Drop-Out Time.	30 30		 20 15	mS	See Waveforms below and Fig.4 VDD = 5V.		
–	TP	Propagation Delay, TOE to L1–L4, H1–H4.			300	nS	VDD = 5V, See Fig.4		



(a) VGT detect level≃1/2 V_{DD}

(b) VGT detect level = V_{REF}

Fig.4 Connections for EST, GT and ST pins

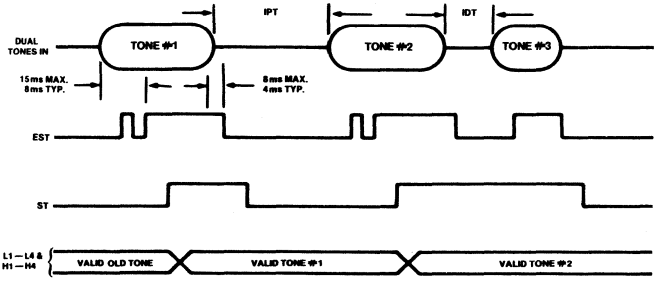


Fig.5 Waveforms

PLESSEY Semiconductors ADVANCE INFORMATION CMOS

MV8865

DTMF FILTER

The MV8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a DTMF Digital Detector (i.e. MV8860/62/63). Switched capacitor techniques are used to implement the filters and the device is fabricated using Plessey Semiconductors' high density technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as an external component. The MV8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

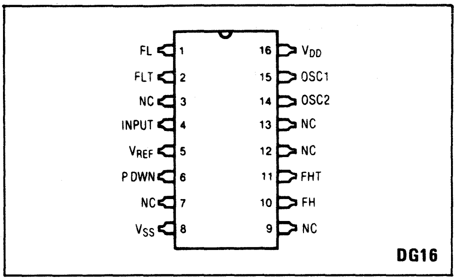


Fig.1 Pin connections (top view)

FEATURES

- Provides DTMF High and Low Group Filtering
- Hard Limiting on Filter Outputs
- 6 Pole Band Pass High and Low Group Filters
- 38 dB Intergroup Attenuation
- Dial Tone Suppression
- +5 to +12 V Single Supply Operation
- Logical Power Down
- Uses Inexpensive 3.58 MHz Crystal
- Wide Dynamic Range 30 dB

APPLICATIONS

In DTMF Receivers for:

- End to End Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

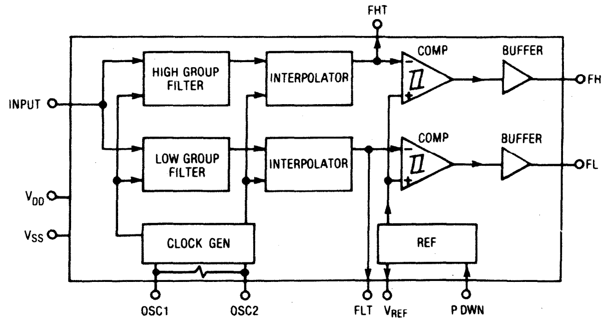


Fig.2 MV8865 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$; $f_{CLK} = 3.579545$ MHz
All voltages wrt V_{SS}

	Characteristic				Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions	
						Min	Typ	Max	Min	Typ	Max			
1	SUPPLY	Operating Supply Voltage			V_{DD}	4.75					13	V		
2		Operating Supply Current			I_{DD}		1.2	2.5		5	7.5	mA	PDWN = V_{SS}	
3		Standby Supply Current			I_{DDS}		100	150		300	400	μA	PDWN = V_{DD}	
4		Operating Power Consumption			P_O		6			60		mW	PDWN = V_{SS}	Fig. 6(c)
5		Standby Power Consumption			P_S		0.5			1.5		mW	PDWN = V_{DD}	C = 15pF
6	INPUTS	Low Level Input Voltage		PDWN & OSC 1	V_{IL}			1.5			3.5	V		
7		High Level Input Voltage			V_{IH}	3.5			8.5			V		
8		Pull Down Sink Current		PDWN	I_{IH}		3	6		12	24	μA		
9		Input Current		OSC 1	I_I		±2.5			± 6		μA		
10	OUTPUTS	Low Level Output Voltage		FL, FH OSC 2	V_{OL}			0.1			0.1	V	No load	
11		High Level Output Voltage			V_{OH}	4.9			11.9			V		
12		Output Drive Current	N Channel Sink	FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)	
13				OSC 2		0.1			0.25			mA	V_{OL} = 1.2V (12V)	
14			P Channel Source	FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)	
15				OSC 2		0.1			0.25			mA	V_{OH} = 10.8V (12V)	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{SS}			15	V
Voltage on any pin		V_{SS} − 0.3	V_{DD} + 0.3	V
Max. current at any pin			10	mA
Operating Temperature		40 °C	+ 85	°C
Storage Temperature	DG package	− 65 °C	+ 150	°C

Parameter		Max
Power Dissipation	DG package[1]	850mW

[1] Derate 16mW/°C above 75°C

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
t_{amb} = +25°C; f_c = 3.579545 MHz; V_{DD} = 4.75 V to 13 V

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1	FILTER	Dynamic Range			30		36	dB		
2		Valid Input Signal Levels					$V_{DD}/2$	V_{pp}		
3		(Each tone of composite signal)			27.9		883	mVrms	V_{DD} = 5V	
4					0.134		4.242	Vrms	V_{DD} = 12V	
5		Input Impedance		Z_i	10			MΩ		
6		Passband Gain		A_V	−1	0	+1	dB		
7		Low Group	Lower Limit	f_{LL}	670	675	679	Hz		
8		1dB Bandwidth	Upper Limit	f_{LU}	964	995	1025	Hz		
9		High Group	Lower Limit	f_{HL}	1150	1162	1178	Hz		
10		1dB Bandwidth	Upper Limit	f_{HU}	1673	1740	1807	Hz		
11		Intergroup	Low Group with	IR_{L1209}	40	45		dB	1209Hz	w.r.t.
12			High Tone	IR_{L1477}	36	40		dB	1477Hz	770Hz
13		Rejection	High Group with	IR_{H941}	40	45		dB	941Hz	w.r.t.
14			Low Tone	IR_{H770}	36	40		dB	770Hz	1336Hz
15		Dial Tone	Low Group	DR_{L440}		60		dB	440Hz	w.r.t
16				DR_{L350}		30		dB	350Hz	770Hz
17		Rejection	High Group	DR_{H440}		60		dB	440Hz	w.r.t.
18				DR_{H350}		50		dB	350Hz	1336Hz
19		FHT FLT Maximum Permissible Load		R_{LFT}	250			KΩ		
20				C_{LFT}			2000	pF		
21	LIM	Output Rise Time	FL, FH	t_{TLHO}		90	150	ns	10% to	
22		Output Fall Time		t_{THLO}		60	100	ns	90% V_{DD}	
23	CLOCK	Crystal/Clock Freq.	OSC 1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz		
24		Clock	Rise Time	t_{LHCI}			110	ns	10% to	Externally
25		Input	Fall Time	t_{HLCI}			110		90% V_{DD}	Applied
26		(OSC 1)	Duty Cycle	DC_{CI}	40	50	60	%		Clock
27		Clock Output OSC 2	Capacitive Load	C_{LOC}			30	pF	Unbalanced load, see Operating Notes	
28		Capacitance Any Input		C_i		5	7.5	pF		

PIN FUNCTIONS

DIP Pin	Name	Description	
1	FL	Low group limiter output.	
2	FLT	Test output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.	
3	NC	Not connected.	
4	INPUT	Tone signal input (single ended).	
5	V_{REF}	Internal reference, can be used to bias input via 2MΩ resistor.	
6	PDWN	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.	
7	NC	Not connected.	
8	V_{SS}	Negative (0V) power supply.	
9	NC	Not connected.	
10	FH	High group limiter output.	
11	FHT	Test output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.	
12	NC	Not connected.	
13	NC	Not connected.	
14	OSC 2	Clock Output.	3.58MHz crystal connected between these pins completes internal oscillator.
15	OSC 1	Clock Input.	
16	V_{DD}	Positive power supply.	

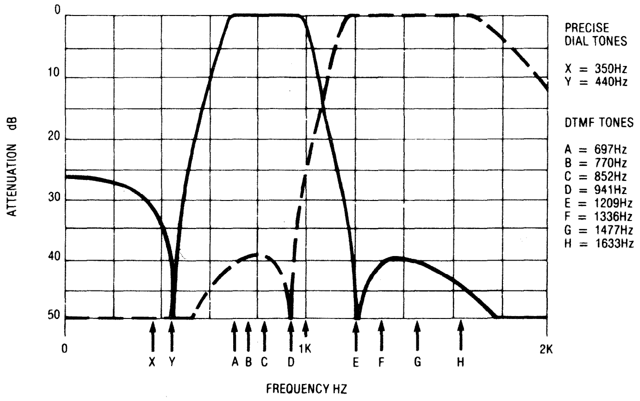


Fig.3 Typical filter characteristics

OPERATING NOTES

The MV8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of one of Plessey Semiconductors' range of DTMF Digital Decoders (MV8820, MV8860/62/63), see Fig.4.

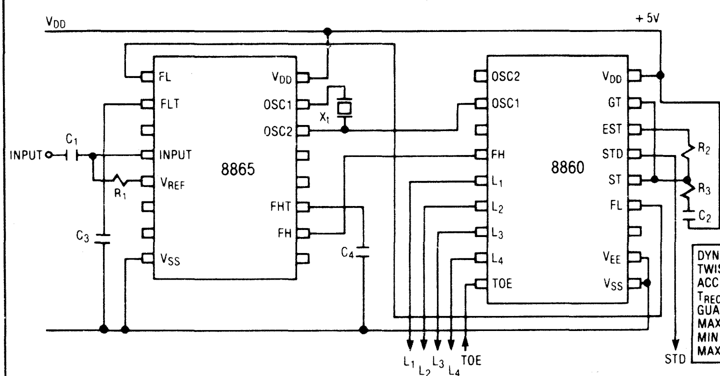
Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig.3) also incorporates a notch at 440 Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting.

The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MV8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig.4) or via a differential buffer to a telephone line (Fig.5). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2 MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680 pF capacitors.

Unbalanced Loads

Presenting a high unbalanced capacitive load to the oscillator crystal can cause Attenuation of the oscillator output signal and increased supply current (see Fig.6). Where the MV8865 oscillator is required to drive a high capacitive load such as a number of other MV8865/8860s it is desirable to connect a capacitor between OSC1 and V_{SS}, the value of this capacitor being equal to the capacitive loading at OSC2.



R_1 = 2.0M
R_2 = 300K
R_3 = 5K
C_1 = 10nF
C_2 = 0.1μF
C_3 = 680pF
C_4 = 680pF
X_t = 3.579MHz

NOTE:

FOR DEVICE POWER SUPPLY >5.25V SEE MV8860 DATA SHEET

TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	25 TO 35ms
GUARD TIME	20ms
MAX. INVALID TONE DURATION	20ms
MIN. INTERDIGIT PAUSE	30ms
MAX. ACCEPTABLE DROPOUT	20ms

Fig.4 Single-ended input receiver using the MV8860 (5 V operation)

DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2$
$R_4 = R_1$
$R_3 = \frac{R_2 R_5}{R_2 + R_5}$

VOLTAGE GAIN

$(A_{V\,diff}) = \frac{R_5}{R_1}$

INPUT IMPEDANCE

$(Z_{indiff}) = 2\sqrt{R_1{}^2 + (\frac{1}{\omega c})^2}$

TYPICAL VALUES

$C_1 = C_2 =$ 10nF
$R_1 = R_4 =$ 200k
R_5 = 100K
R_2 = 50K
R_3 = 37.5K
$A_{V\,diff}$ = − 6dB
Z_{indiff} ≃400KΩ (@ 650Hz)

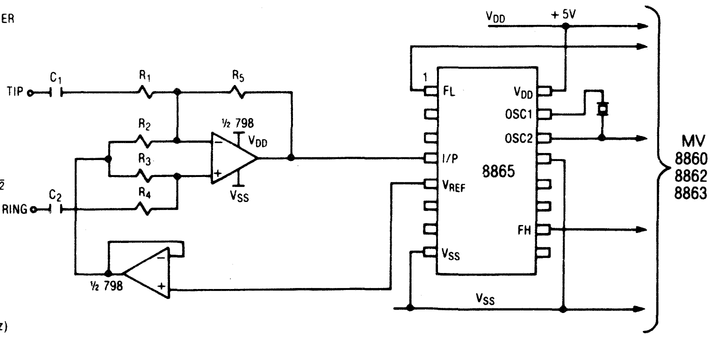


Fig.5 Connection to a telephone line

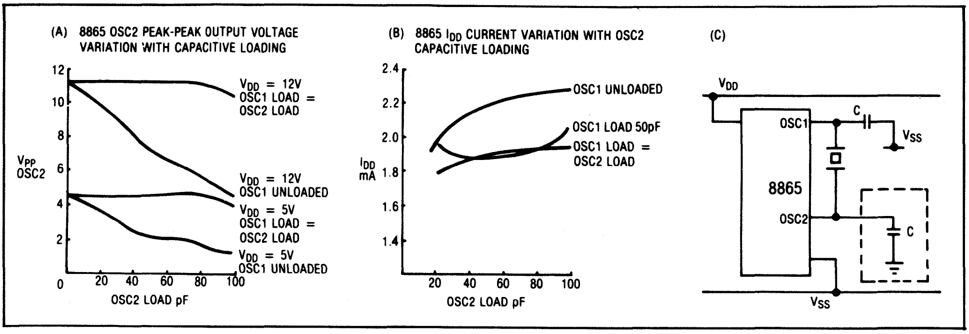


Fig.6 Crystal oscillator loading

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL792

CAPACITANCE MICROPHONE AMPLIFIER (PVDF)

The amplifier is intended for use with any microphone requiring a high input impedance and having a capacitance of 330pF or more (i.e. PVDF type). Gain adjustment of 13dB is provided by means of external links and external resistors. The gain range and input impedance of the SL792 is matched to the requirements of Polyvinylidene Fluoride (PVDF) film transducers. Low frequency roll-off is controlled with an external capacitor. The device operates from either polarity supply and closely simulates the DC characteristics of a carbon microphone.

When used with an appropriate transducer the device conforms to BPO specifications S1377 (July 1978): 'A linear microphone replacement for transmitter replacement No.16.

OPERATING NOTES

1. The amplifier will operate with either polarity supply.
2. A series capacitor of at least 330pF is required if a low impedance microphone is used.
3. The external 22ohm resistor is required to meet PO specification and is not otherwise needed.

The LF roll-off may be calculated from

$$f = \frac{1}{2\pi CR}$$

where R = 160ohms, See Fig 4

4. Secondary surge protection is necessary to meet the requirements of most PTTs. This should be placed across the terminals of the assembly, as shown in Fig 4.

Suitable devices are:

Zener diodes : BZX87C15

Varistor voltage suppressors : G.E.V18ZA 1
National ERZCO7DK/80

Transorbs by General Semiconductor
Industries : P6KE18

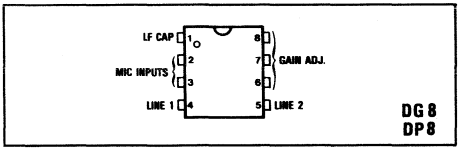

Fig.1 Pin connections

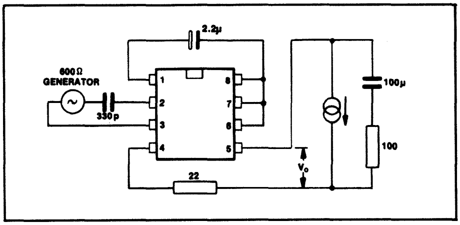

Fig.2 Test circuit

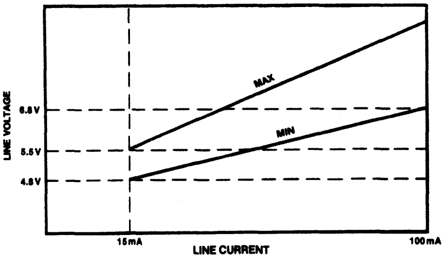

Fig.3 Supply characteristics

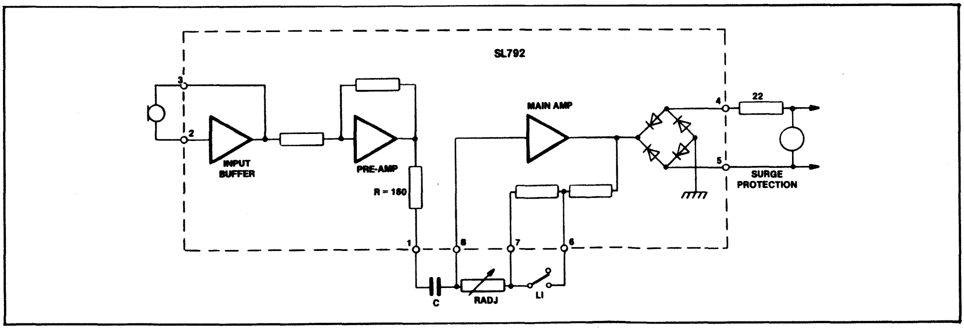

Fig.4 Block diagram/surge protection

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Line current, 50mA
Ambient temperature, +22°C ± 3°C
Test circuit: Fig 2
Freq = 1kHz at 240mV rms O/P

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	**Typ.**	**Max.**		
Gain nominal	G		38	40	42	dB	See Fig.2
Gain adjustment range relative to G			+13			dB	See Fig.6
Gain adjustment tolerances (over complete range)			-0.3		+0.3	dB	See Fig.2 & 6
Gain variation with temp. -10°C to +50°C relative to G				±1.0		dB	See Fig.2 at 710mV O/P
Gain at 300Hz rel.G			-10.5		-5.4	dB	See Fig.5
Gain at 3.4kHz rel.G					+3	dB	See Fig.5
Gain change from 100mA to 50mA			-0.5		+0.5	dB	See Fig.7
Gain change from 50mA to 20mA			-0.5		+0.5	dB	See Fig.7
Gain change from 50mA to 10mA			-10	-1	+0.5	dB	See Fig.7
Noise(psophometric)					-74	dBvP	At 40dB gain
Harmonic distortion	THD			4.5	5.5	%	At 710mV O/P signal
				1.8	2.5	%	At 240mV O/P signal
Signal handling capability	V_{out}				710	mV rms	See Fig.2
Terminal voltage	$V_{4\,5}$	4,5	4.8		5.5	V	At 15mA Fig.3
			6.8		12.2	V	At 100mA Fig.3
Operating current	$I_{4\,5}$	4,5	10		120	mA	See Fig.3
Input impedance	Zin	2,3	1.6	2.5		Mohms	
Output impedance	Zout	4,5			25	ohms	Excluding 22ohms series resistor Fig.2
Gain change with polarity					0.5	dB	At 710mV O/P

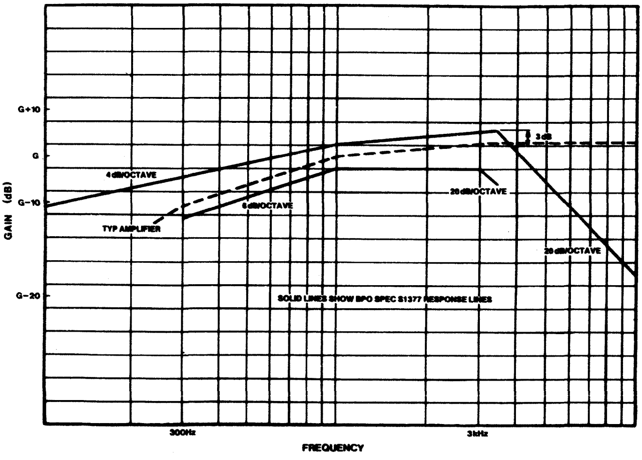

Fig.5 Frequency response of test circuit shown in Fig.2

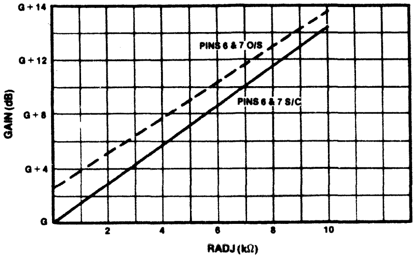

Fig.6 Gain adjustment v. Radj

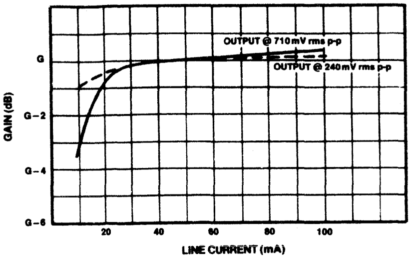

Fig.7 Gain v. line current (typical)

ABSOLUTE MAXIMUM RATINGS

Operating temperature range: -10°C to +50°C
Max. current (pins 4,5): 250mA for 20 seconds
Thermal resistance (chip-to-ambient):
130°C/W (DP8, DG8)

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PRELIMINARY INFORMATION

Preliminary Information is issued to advise Customers of potential new products which are designated '*Experimental*' but are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to current or future availability. Customers incorporating '*Experimental*' product into their equipment designs do so at their own risk. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL793

CAPACITANCE MICROPHONE AMPLIFIER (ELECTRET)

The amplifier is intended for use with any microphone requiring a high input impedance and having a capacitance of 33pF or more (i.e. electret type). Gain adjustment of 6dB is provided by means of external links and external resistors. The gain range and input impedance of the SL793 is matched to the requirements of electret film transducers. Low frequency roll-off is controlled with an external capacitor. The device operates from either polarity supply and closely simulates the DC characteristics of a carbon microphone.

When used with an appropriate transducer the device conforms to BPO specifications S1377 (July 1978): A linear microphone replacement for transmitter replacement No.16.

OPERATING NOTES

1. The amplifier will operate with either polarity supply.
2. A series capacitor of at least 33pF is required if a low impedance microphone is used.
3. The external 15ohm resistor is required to meet PO specification and is not otherwise needed.

The LF roll-off may be calculated from

$$f = \frac{1}{2\pi CR}$$

where R = 160ohms See Fig 4.

4. Secondary surge protection is necessary to meet the requirements of most PTTs. This should be placed across the terminals of the assembly, as shown in Fig 4.

Suitable devices are:

Zener diodes : BZX87C15

Varistor voltage suppressors : G.E.V18ZA 1
National ERZCO7DK/80

Transorbs by General Semiconductor
Industries : P6KE18

5. The gain, G of the microphone amplifier can be calculated from the following formula:

$G = 20 \text{ Log}_{10} (4.93(\text{Radj}+\text{RT}) +10)$

Where RT is the gain trim resistor, see Fig 4.
(RT = 0.24kΩ nominal)

ABSOLUTE MAXIMUM RATINGS

Operating temperature range: -10°C to +50°C
Max. current (pins 4,5): 250mA for 20 seconds
Thermal resistance (chip-to-ambient):
130°C/W (DP8),(DG8)

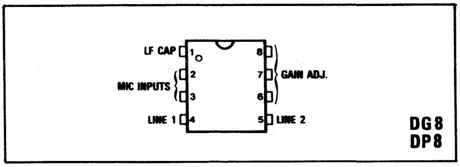


Fig.1 Pin connections

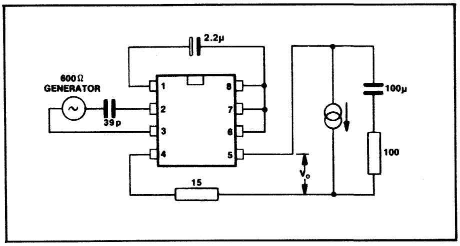


Fig.2 Test circuit

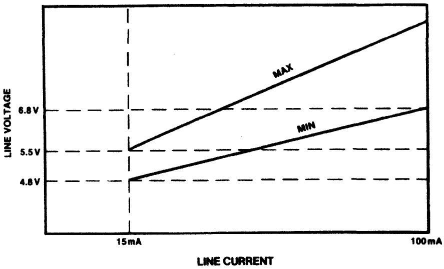


Fig.3 Supply characteristics

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Line current at 50mA
Ambient temperature +22°C ± 3°C
Test circuit: Fig 2
Freq = 1kHz at 240mV rms O/P

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Gain nominal	G		18	20	22	dB	See Fig.2
Gain adjustment range relative to G			+6			dB	See Fig.6
Gain adjustment tolerances (over complete range)			-0.3		+0.3	dB	See Fig.2 & 6
Gain variation with temp. -10°C to +50°C relative to G				±1.0		dB	See Fig.2 at 710mV O/P
Gain at 300Hz rel.G			-10.5		-5.4	dB	See Fig.5
Gain at 3.4kHz rel.G					+3	dB	See Fig.5
Gain change from 100mA to 50mA			-0.5		+0.5	dB	See Fig.7
Gain change from 50mA to 20mA			-0.5		+0.5	dB	See Fig.7
Gain change from 50mA to 10mA			-10	-1	+0.5	dB	See Fig.7
Noise(psopho-metric)					-80	dBvP	At 20dB gain
Harmonic distortion	THD			4.5	6	%	At 710mV O/P signal
				1.8	3	%	At 240mV O/P signal
Signal handling capability	V_{out}				710	mV rms	See Fig.2
Terminal voltage	$V_{4\ 5}$	4,5	4.8		5.5	V	At 15mA Fig.3
			6.8		12.2	V	At 100mA Fig.3
Operating current	$I_{4\ 5}$	4,5	10		120	mA	See Fig.3
Input impedance	Zin	2,3	6			Mohms	
Output impedance	Zout	4,5			25	ohms	Excluding 15ohms series resistor Fig.2
Gain change with polarity					0.5	dB	At 710mV O/P

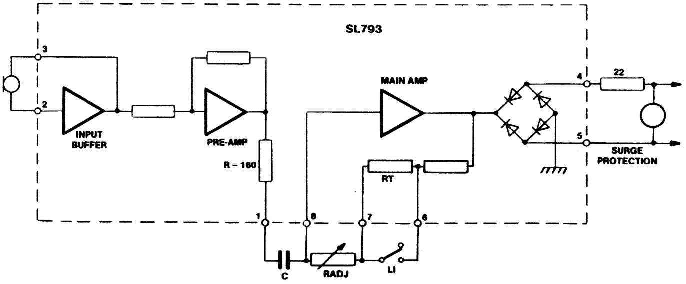
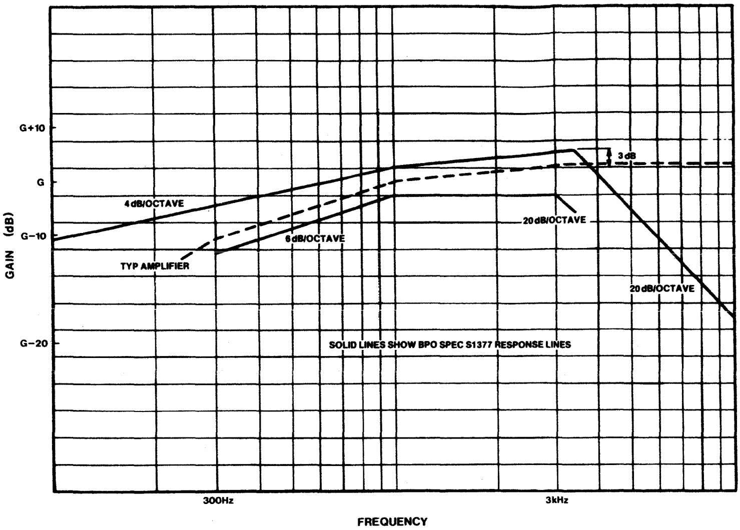


Fig.4 Block diagram/surge protection



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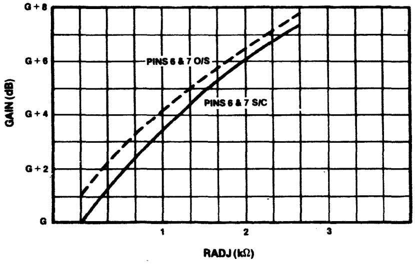

Fig.6 Gain adjustment v. Radj

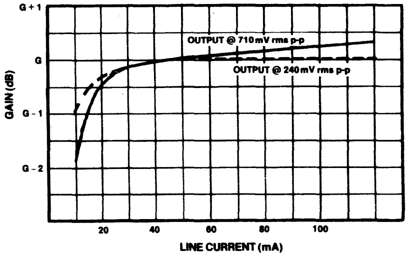

Fig.7 Gain v. line current (typical)

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SL1001A

MODULATOR/DEMODULATOR

The SL1001A is a bipolar monolithic integrated circuit double balanced modulator, designed primarily for use in telephone transmission equipment, but equally suitable for any application where the modulation function is required.

The device employs conventional 'tree' configuration multiplier circuits. Careful design of the circuit layout results in low carrier and signal leak levels, with high dynamic range and good linearity. Internal bias is provided, allowing direct balanced transformer input, or single-ended capacitor drive.

A two-stage common collector output structure is used to provide a low output impedance.

A pair of diodes is included to provide optional carrier input limiting.

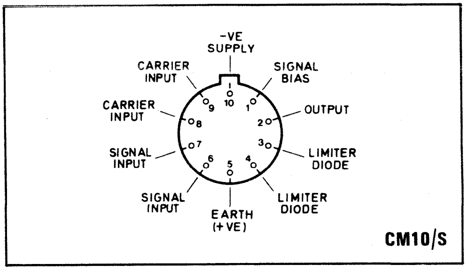


Fig.1 Pin connections (bottom)

FEATURES

- High Carrier and Signal Suppression: 50dB
- Unity Conversion Gain
- Low Noise Level: −112dBmp
- High Intermodulation Suppression: 58dB
- Low Supply Current: 6mA
- Diodes Included for Limiting

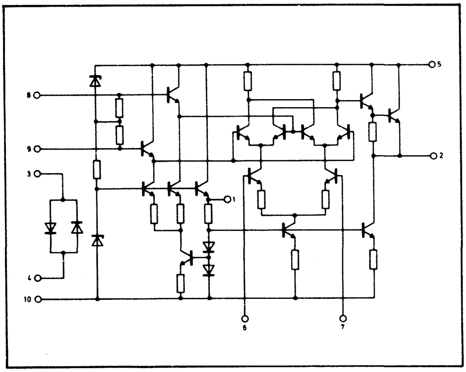


Fig.2 Circuit diagram

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- FM Detection
- Phase Detection

QUICK REFERENCE DATA

Supply Voltage	−15V
Supply Current SL1001A	6mA
Carrier Level	125mVrms (Min.)
Signal Level	Up to 600mVrms
Output Current SL1001A	3.5mA peak (Typ.)
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C
Circuit ref: Figs.3 and 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Conversion gain	− 1	0	+1	dB	
Signal input impedance		150		kΩ	Pins 6 & 7
Carrier input impedance	7	10	13	kΩ	Pins 8 & 9
	3.3	5	6.7	kΩ	Pins 8 & 5 or 9 & 5
Output impedance		12		Ω	Pin 2
Signal suppression	20	50		dB	Signal 170mV, Carrier 500mV
Carrier suppression	20	40		dB	
2nd harmonic suppression		40		dB	
Carrier compression			0.1	dB	For ± 3dB on 500mV
Supply line suppression		50		dB	Supply line resistance=500Ω
Sig. and carrier band width	200			kHz	
Carrier level	125			mVrms	
Signal level			600	mVrms	
Output current		3.5		mApk	
Noise level		− 112	− 105	dBmp	Weighted speech band
Intermod. products		− 58		dB	Signals 2 X 170mV
Gain stability		0.12		dB	+5°C to +55°C
		0		dB	± 10% supply
Adjusted carrier suppression		70		dB	See Fig.5

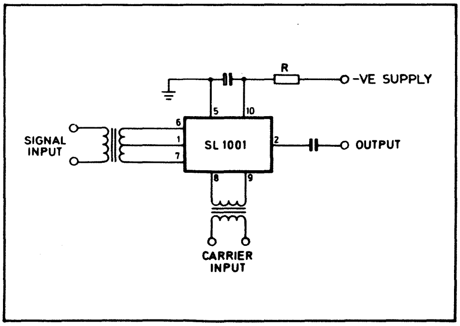


Fig.3 Transformer input

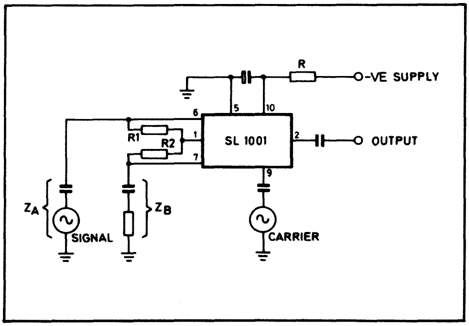


Fig.4 Unbalanced input

OPERATING NOTES

1. A resistance in series with the supply (Pin 10) is usually advisable, to improve the supply rejection and reduce the circuit voltage.
2. For good carrier suppression, the signal input bias resistors should be equal and have a value less than 5kΩ
3. For improved intermodulation suppression, Pin 1 may be decoupled, preferably with a 100Ω resistor in series with Pin 1.

   If Pin 1 is not decoupled, noise is optimised when an unbalanced drive is used, by providing equal source impedances for Pins 6 and 7.
4. Low leakage input capacitors are advisable for the input connections to avoid inducing carrier or signal leakage.
5. Carrier suppression may be improved by using the circuit of Fig.5, and adjusting for minimum leakage.
6. This device is also available with tin-dipped leads, order as SL1001AM.

OPERATING CONDITIONS (see Figs.3 and 4)

Parameter	Value	Units	Condition
Supply voltage	−15	V	Pin 10
Supply current	6	mA	
Input bias current	5	μA	Pins 6 & 7
Dynamic resistance	8	kΩ	Pins 5 to 10
Output quiescent voltage	−3	V	Pins 2 to 5
Temperature range	−25 to +125	°C	

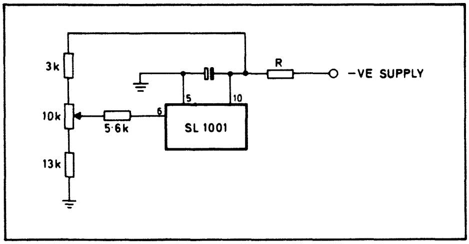


Fig.5 Carrier suppression adjustment

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 820Ω)	−30V
Storage temp. range	−55°C to + 175°C
Free air operating temp. range	−40°C to + 150°C

PLESSEY
Semiconductors

SL1021 A & B

CHANNEL AMPLIFIER

The SL1021 A and B are bipolar monolithic integrated circuit amplifiers designed for use as channel amplifiers in telephone transmission equipment and satisfy the requirements of the British Post Office channel translating apparatus (RC5467).

The two variants A and B are distinguished by guaranteed output levels of +10dBm and +13dBm, respectively, other parameters being identical.

The main feature of these devices is the provision of a temperature-stable DC operated remote gain control facility having an adjustable range of control.

The connections provided allow a variety of uses, including fixed gain amplification with various feedback configurations.

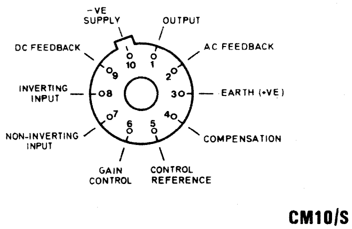
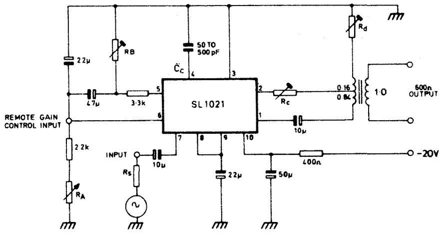


Fig. 1 Pin connections

FEATURES

- Up to +13dBm O/P into 600Ω (Class A)
- Temperature insensitive remote DC gain control
- Non-interactive adjustment of:
  - Gain
  - Gain Range
  - Output Return Loss
- 1:1 600Ω Transformer output can be optimized for low inductance using 2-element filter configuration
- Power Bandwidth: 150kHz (fixed gain, Fig. 4)
- Small Signal gain Bandwidth: 3MHz (see Fig. 4)



TEST CONDITIONS

R_A = 3·9kΩ
R_B = ADJUST FOR 7·4dB GAIN RANGE (≈3k)
R_C = 0
R_s = 0 TO 600Ω
Rd = ADJUST FOR MIN. RETURN LOSS (≈75Ω)
C_C = 50 – 500pF
GAIN = 26dB

Fig. 2 SL1021 test circuit and typical application

APPLICATIONS

- Telephone Communications
- Channel Group Translation Equipment
- Radio – communications
- Small Signal Processing

QUICK REFERENCE DATA

Supply Voltage	–20V (via 400Ω)
Supply Current	9mA
Gain Control Current	0.5mA
Temperature Range	–25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C

These characteristics are those obtained using the test circuit of Fig. 2, the gain range and output impedance being adjusted as indicated.

Characteristics	Value			Units	Conditions
	Min.	Typ,	Max.		
Gain (reference gain G)	24.5	26	27.5	dB	
Gain/R_S			28	dB	R_S = 600Ω to 3kΩ
Gain range		7.4		dB	Adjusted
Gain law					
R_A = 125Ω	3.9	4.1	4.3	dB	Relative to G
R_A = 9kΩ	−3.5	−3.3	−3.1	dB	
Gain/temperature	−0.1		+0.1	dB	Relative to G, T = 10°C to 45°C
Gain/V_S			0.1	dB	V_S = −20V ± 1V
Distortion					
2nd harmonic			−36	dBm0	At 10dBm output
3rd harmonic			−45	dBm0	
Overload					
SL1021A	10	13		dBm	Class A operation
SL1021B	13	15		dBm	
Noise			−76	dBmP	Proportional to G
Output impedance		600		Ω	Adjusted
Return loss	20			dB	250Hz to 3.4kHz
Input impedance	10			kΩ	Variable with R_A and R_S
Gain at reduced V_S	25.5			dB	V_S = −17.5V See Fig.2
Overload at reduced V_S	7			dBm	V_S = −17.5V
Gain control interaction between channels (change in gain for 3.3 mA current change)			0.25	dB	Equivalent to 11 channels, Common R_A earth return
Frequency response	240		3400	Hz	±0.05dB ref. 800Hz
Bandwidth			100	kHz	C_C = 50pF

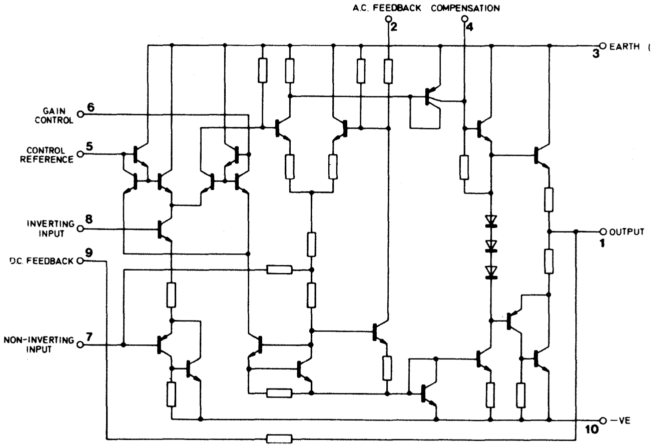


Fig. 3 SL1021 equivalent circuit

OPERATING CONDITIONS (see Fig. 2)

Parameter	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11.0	mA	$R_A = 0$
		7.0		mA	$R_A = 11k\Omega$
Supply voltage		–20		V	Via 400Ω
Supply voltage on chip		–17		V	Pin 10
Supply maximum			–23	V	Pin 10
Control current		0.5		mA	$R_A = 0$
		0.26		mA	$R_A = 10k\Omega$
Control current change			0.3	mA	$R_A = 0$ to $11k\Omega$
Operational temp.	–25		+125	°C	
Fixed gain application (see Fig. 4)					
Optimum load		100		Ω	
Power output		20		mW	Class AB
Power bandwidth		150		kHz	10mW
Gain		20		dB	Values as Fig. 4
Frequency response		3		MHz	Small signal

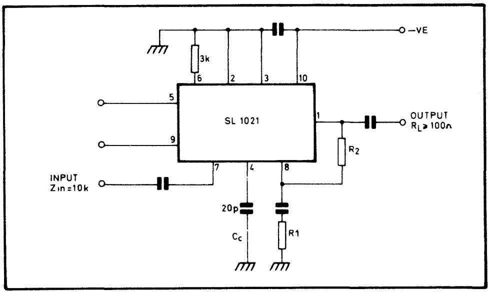


Fig. 4 Fixed gain amplifier, Class A or AB

OPERATING NOTES

1. The control decoupling capacitors should be of a low leakage type.
2. Other values of control resistors are possible if other gains/gain ranges are required. However, the parallel resistance to earth from pins 5 and 6 should be ≤8kΩ at all settings.
3. If the control resistance is increased or open circuited, the amplifier gain will decrease to zero. (See Fig. 4 for fixed gain use).
4. The compensation capacitor can be increased to reduce the frequency response and power bandwidth.
5. The gain may be increased from the value of Fig. 2 (26dB nominal) by increasing R_c, the gain increase being given by:

$$\frac{R_c + 8.5}{8.5} \pm 20\%$$

where R_c is in kΩ.

Because of temperature coefficient mismatch between R_C and internal resistors, the gain stability may be degraded with temperature.

6. The case is connected to pin 10 (–ve supply). To avoid damage to the device when operating with a positive earth system, care should be taken to prevent the case from becoming earthed.
7. This device is also available with tin-dipped leads, order as SL1021AM.

ABSOLUTE MAXIMUM RATINGS

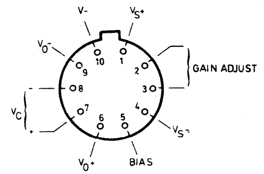
Supply voltage (via 400Ω)	–30V
Storage temp. range	–55°C to +175°C
Free air operating temp. range	–40°C to +130°C

PLESSEY
Semiconductors

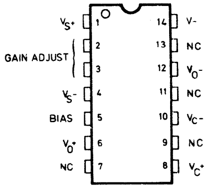
SL1496C SL1596C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1596C and SL1496C are versatile monolithic integrated circuit double balanced modulators/ demodulators, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1596 has an operating temperature range of –55°C to +125°C, whilst that of the SL1496 is 0°C to +70°C.



CM10



DG16 DP16

FEATURES

- Carrier Suppression 65dB Typ. @ 500 kHz; 50dB Typ. @ 10 MHz
- Common Mode Rejection 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Telephone FDM Systems

ORDERING CODES

SL1496C — CM, SL1496C — DG, SL1496C — DP
SL1596C — CM, SL1596C — DG

ABSOLUTE MAXIMUM RATINGS

(Pin number reference to CM package)

Applied voltage*	30V
Differential input signal (V_7—V_8)	±5V
Differential input signal (V_4—V_1)	± (5+15R_E)V
Bias current (I_5)	10mA
Operating temperature range	
SL1496	0 °C to +70 °C
SL1596	—55 °C to +125 °C

CM Package

Storage temperature range	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	680mW

DG Package

Storage temperature range	—55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	600mW

DP Package

Storage temperature range	—55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation (25 °C)	500mW

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):–

V^+ = +12V DC, V^- = –8V DC, I_5 = 1.0 mA DC, R_L = 3.9 kΩ, R_e = 1.0 kΩ T_A = +25°C
All input and output characteristics single-ended, unless otherwise stated.

Characteristic*	SL1596			SL1496			Units
	Min	Typ	Max	Min	Typ	Max	
Carrier Feedthrough							µV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz	–	40	–	–	40	-	
offset adjusted to zero f_C = 10 MHz	–	140	–	–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz	–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz	–	20	100	–	20	200	
Carrier Suppression							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave	50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave	–	50	–	–	50	–	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\|V_C\|$ = 0.5 V DC	2.5	3.5	–	2.5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance	–	200	–	–	200	–	kΩ
Parallel Input Capacitance	–	2.0	-	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance	–	40	-	–	40	–	kΩ
Parallel Output Capacitance	–	5.0	–	–	5.0	–	pF
Input Bias Current $\frac{I_1 + I_4}{2}$; $\frac{I_7 + I_8}{2}$	–	12	25	–	12	30	µA
Input Offset Current $(I_1 - I_4)$, $(I_7 - I_8)$	–	0.7	5.0	–	0.7	7.0	µA
Average Temperature Coefficient of Input Offset Current (T_A = –55°C to +125°C)	–	2.0	-	–	2.0	–	nA/°C
Output Offset Current $(I_6 - I_9)$	–	14	50	–	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = –55°C to +125°C)	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 V DC	–	85	–	–	–85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	–	8.0	–	–	8.0	–	V DC
Differential Output Voltage Swing Capability	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current							mA DC
$I_6 + I_9$	–	2.0	3.0	–	2.0	4.0	
I_{10}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	–	33	–	–	33	–	mW

*Pin numbers are given for TO-5 package.

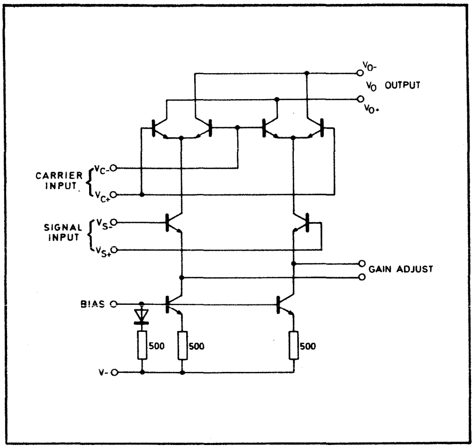


Fig. 2 ***Circuit diagram***

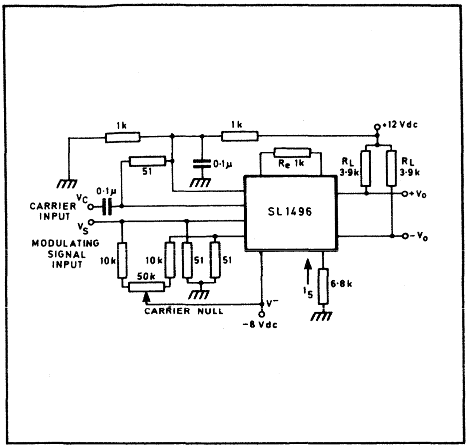


Fig. 3 ***Typical modulator circuit***

PLESSEY
Semiconductors

SP1404BW

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

CIRCUIT DESCRIPTION (FIG. 2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs an inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to ($V_{CC}-1$) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

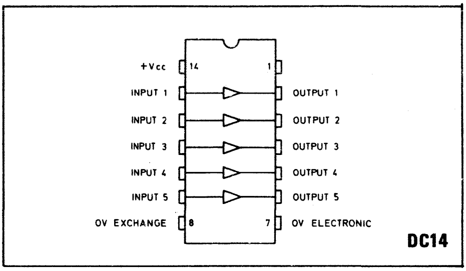


Fig. 1 Pin connections (viewed from underside)

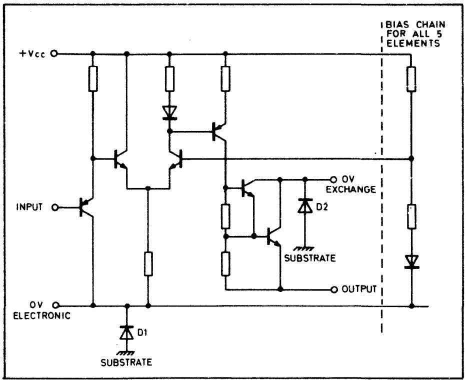


Fig. 2 Circuit diagram of one element

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
Temperature range = 0°C to +70°C
V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		−20		μA	V_{in} = 0V
		−2		μA	$V_{in} = V_{cc}$
Output voltage			1.5	V	V_{in} = 0.8V, I_{out} = 50mA
Output current (Off state)			100	μA	V_{in} = 2V, V_{out} = -60V
Output current (On state)	50	80		μA	Vin = 0.8V
V_{CC} supply current		30		mA	V_{cc} = 5V, all inputs low
Total power dissipation		450		mW	V_{cc} = 5V, all inputs low all outputs I_{out} = 50mA

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{out} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy' earth	–65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

PLESSEY
Semiconductors

SP1450B(B) & SP1455B(B)

PCM SIGNAL MONITOR CIRCUITS

The SP1450 and SP1455 are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

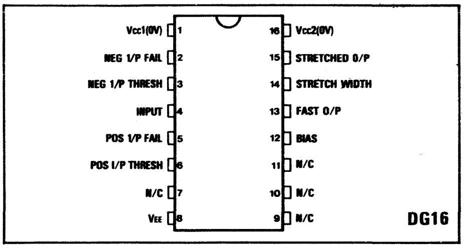


Fig.1 Pin connections (top view)

FEATURES

- Suitable for 34, 120 and 140M bit/s PCM
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature Range -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

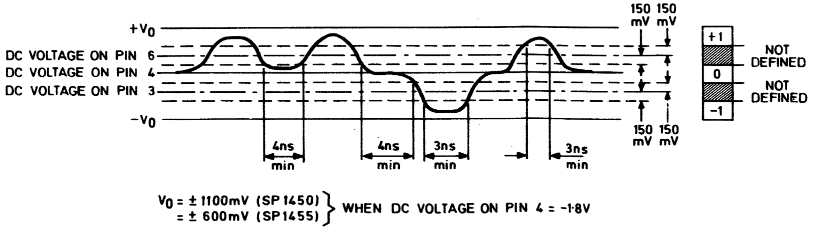


Fig.2 Input pulse wave form

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = Pins 1-16 = 0V
V_{EE} = Pin 8 = -5.0V
T_{amb} = +25°C
Input voltage range (pins 3,4,6) = -0.9V to -3.1V

DC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output low, current	2	0.9	1.2	1.9	mA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2.0V
Output low, current	2	0.7	—	—	mA	Pin 2 = OV Pin 3 = —1.95V Pin 4 = —2.0V
Output high, current	2	—	—	1	µA	Pin 2 = OV Pin 3 = —2.3V Pin 4 = —2.0V
Output high, current	2	—	—	0.4	mA	Pin 2 = OV Pin 3 = —2.05V Pin 4 = —2.0V
Output low, current	5	0.9	1.2	1.9	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.3V
Output low, current	5	0.7	—	—	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.05V
Output high, current	5	—	—	1	µA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.7V
Output high, current	5	—	—	0.4	mA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.95V
Output low, current	13	6.0	7.0	9.0	mA	Pin 13,15 = OV Pin 3 = —1.7V Pin 4 = —2.0V Pin 6 = —2.3V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V Six pos. or neg. pulses on pin 4
Output high, current	15	—	—	1	µA	
Output high, current	13	—	—	1	µA	Pin 13, 15 = OV Pin 3 = —2.3V Pin 4 = —2.0V Pin 6 = —1.7V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V
Output low, current	15	0.5	0.75	—	mA	
Current consumption	1,16	—	20	25	mA	(Pins 2,5,13,15 = OV (Pins 3,6 = —2.3V (Pin 4 = —2.0V (27 kΩ resistor between (Pin 14 and —5V (Pin 12 open
Input bias current	3	—	—	40	µA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2V
Input bias current	6	—	—	40	µA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —1.7V
Input bias current	4	—	—	80	µA	Pins 2,5 = OV Pins 3,6 = —2.3V Pin 4 = —2.0V

AC CHARACTERISTICS

Circuit reference: Fig.3
Input signal: Fig.2
T_{amb} = -10°C to +70°C
V_{EE} = -4.4V to -5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Input Frequency						
SP1450	13		—	25.5	M band/s	See note 1 below
SP1455	13		—	105	M band/s	See note 1 below
Stretched output pulse width	15	0.5	0.7	2	µS	c_1 = 390 pF R_1 = 27 kΩ using circuit of Fig. 7 (see note 2 below)
Error pulse width SP1455	13	4.25	—	5.25	nS	Input freq. 105 M band/s
Error pulse amplitude	13	300	—	—	mV	At max input frequency
Spurious pulse amplitude	13	—	—	50	mV	At max. input frequency

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).

NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

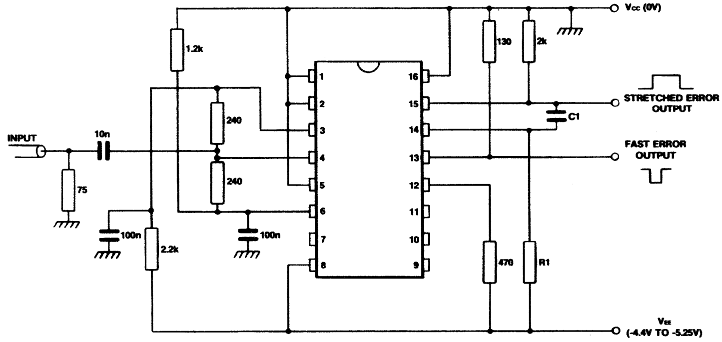


Fig.3 Functional test circuit

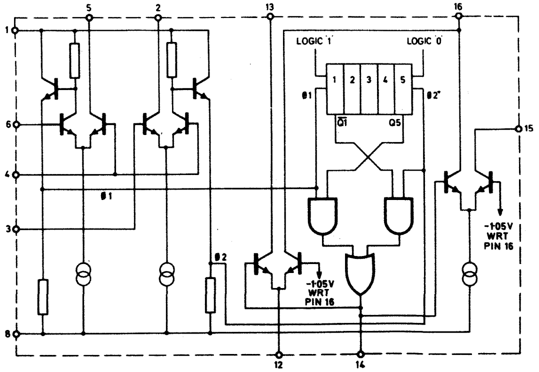


Fig.4 Circuit diagram of SP1450/SP1455

APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' (V_{EE}) to '1' (V_{CC}). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

State	1	2	3	4	5
A	0	0	0	0	0
B	1	0	0	0	0
C	1	1	0	0	0
D	1	1	1	0	0
E	1	1	1	1	0
F	1	1	1	1	1

Fig.5 Shift register states

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and V_{EE} according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and V_{CC} to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to V_{CC} (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to V_{CC} (pin 1). A CMOS interface circuit is shown in Fig.8.

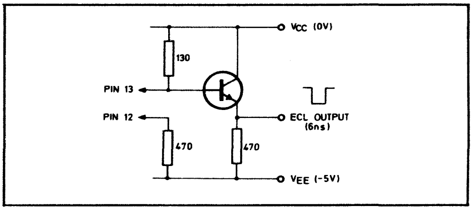


Fig.6 Interfacing with ECL at the output

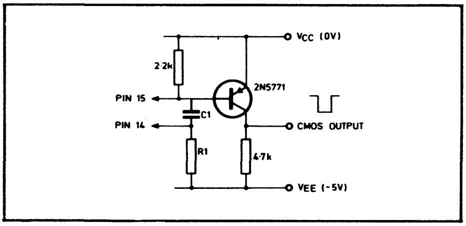


Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)

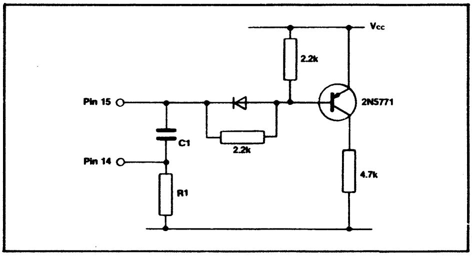


Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)

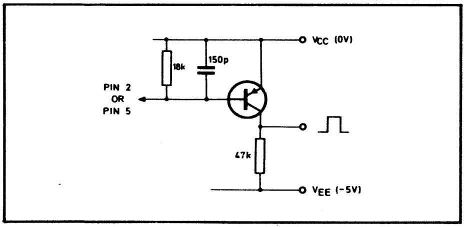
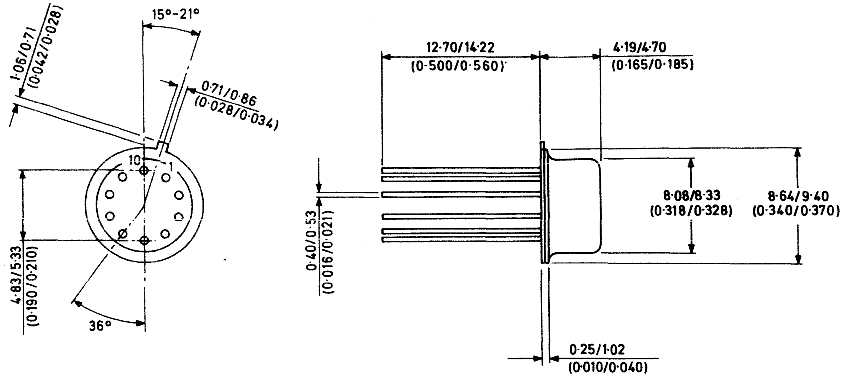


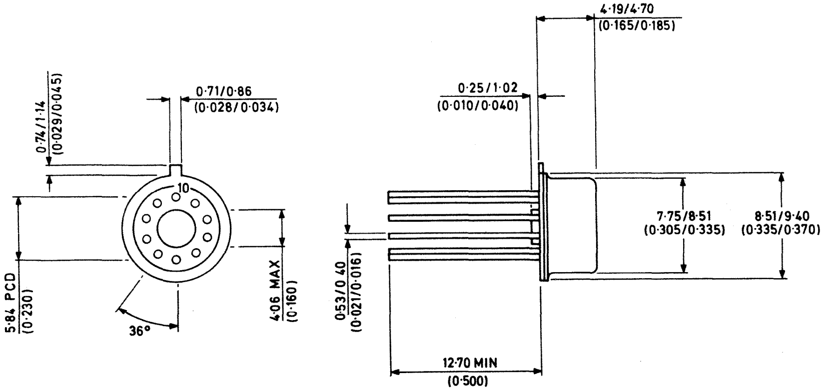
Fig.8 Interfacing with pulse fail output with CMOS

Package Outlines



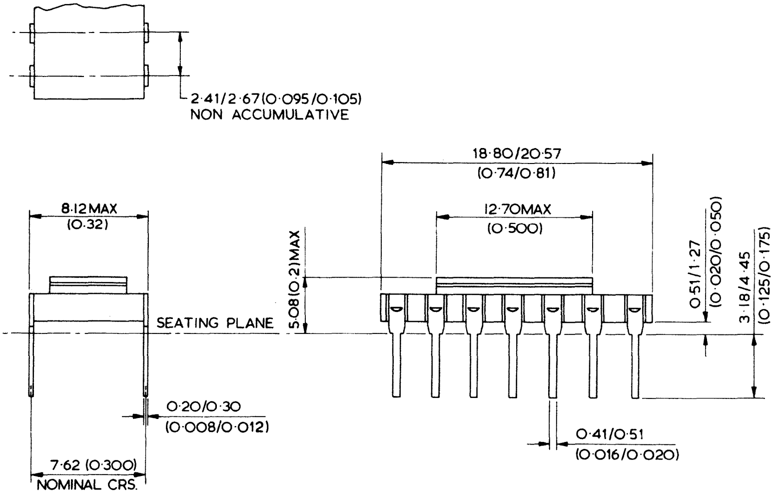
10 LEAD TO-5

CM10



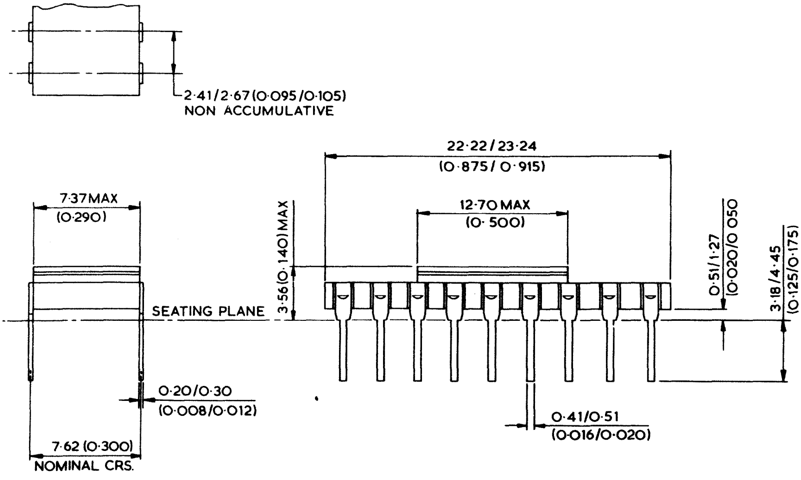
10 LEAD TO-100 (5.84mm PCD) WITH STANDOFF

CM10/S



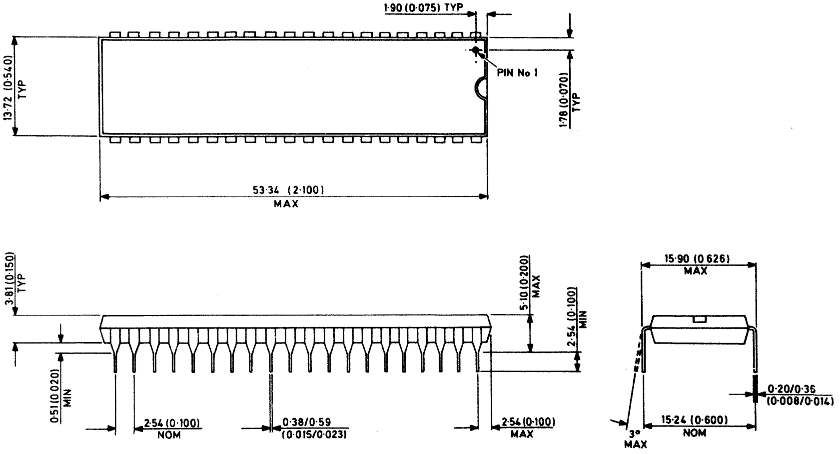
14 LEAD DILMON

DC14



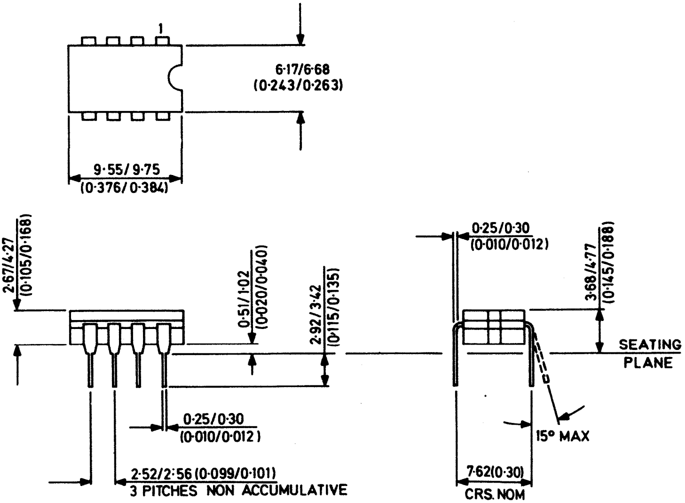
18 LEAD DILMON

DC18



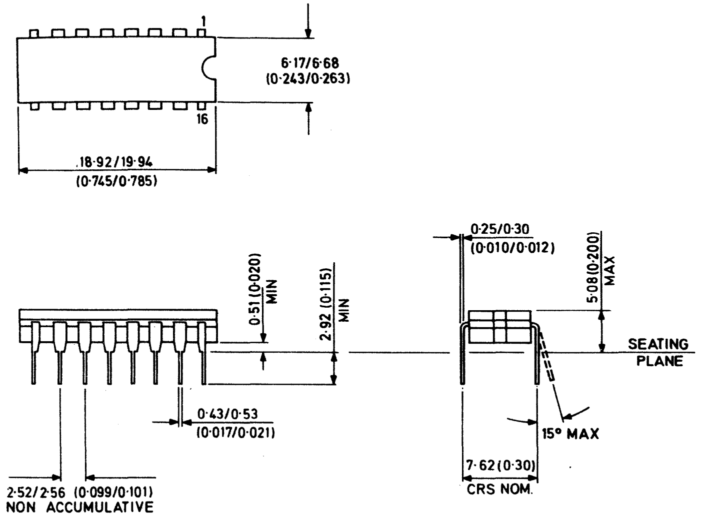
40 LEAD (SIDE BRAZED) DIL

DC40



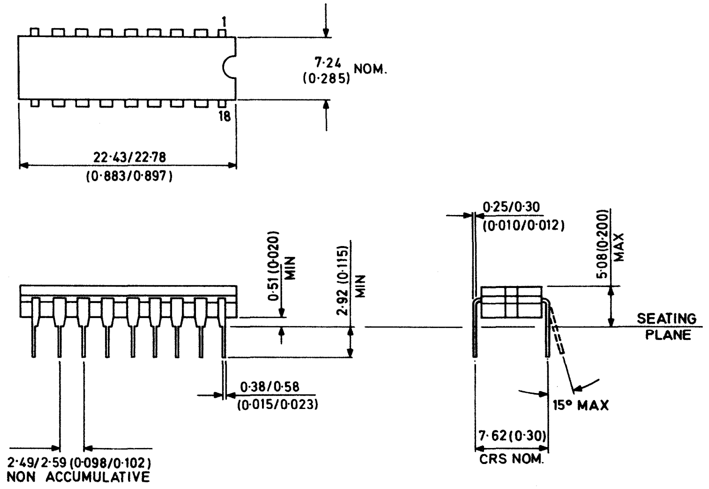
8 LEAD CERAMIC DIL

DG8



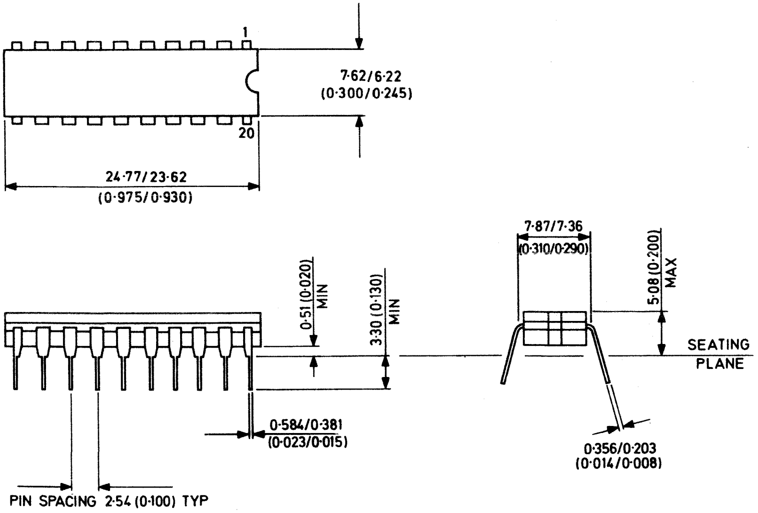
16 LEAD CERAMIC DIL

DG16

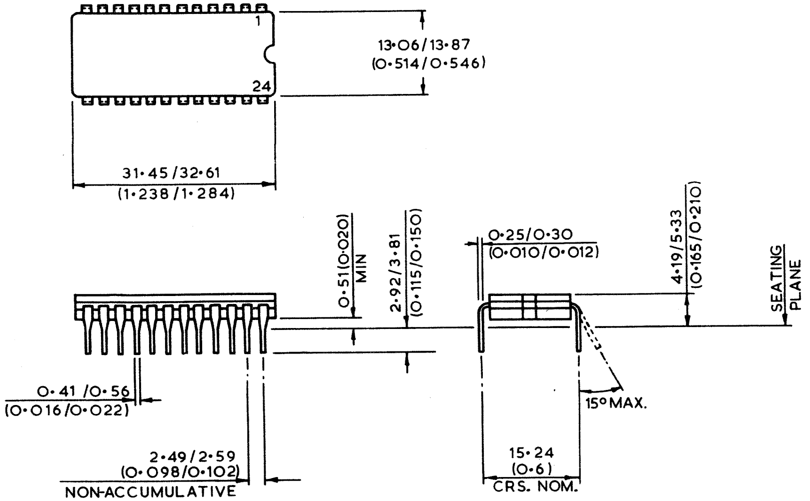


18 LEAD CERAMIC DIL

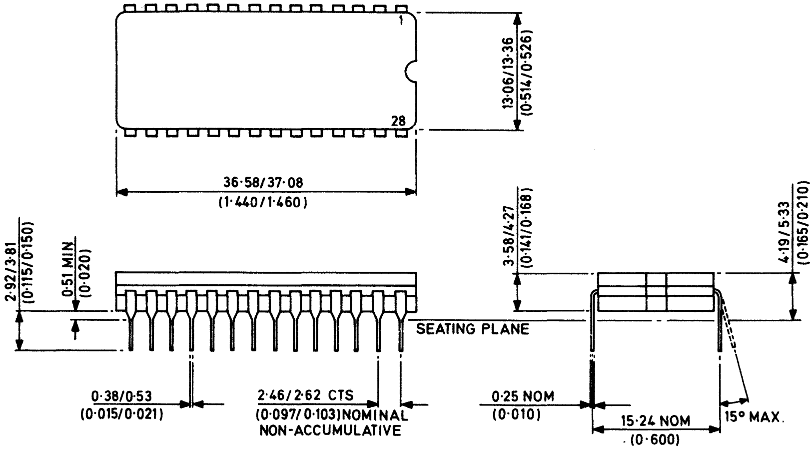
DG18



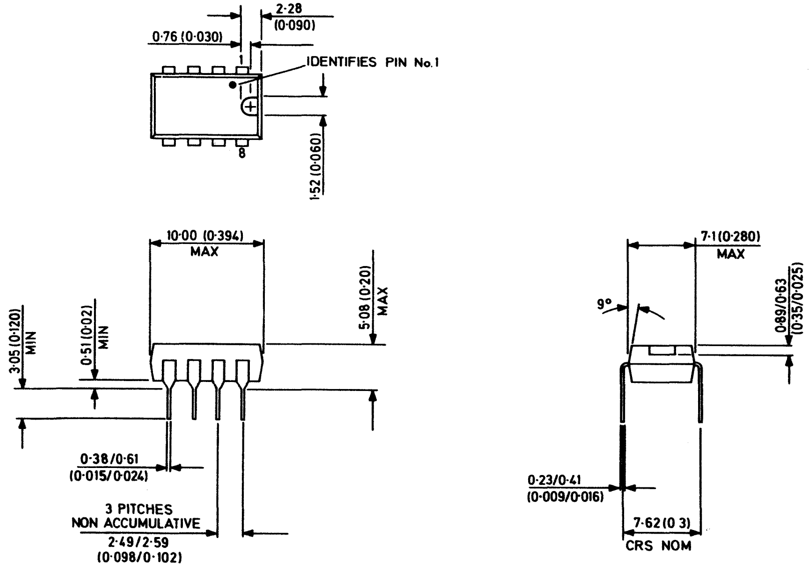
20 LEAD CERAMIC DIL **DG20**



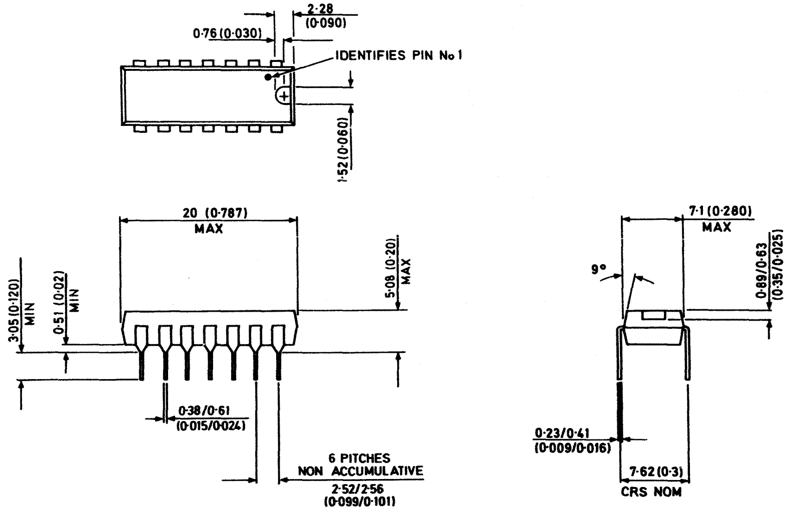
24 LEAD CERAMIC DIL **DG24**



28 LEAD CERAMIC DIL **DG28**



8 LEAD PLASTIC DIL **DP8**



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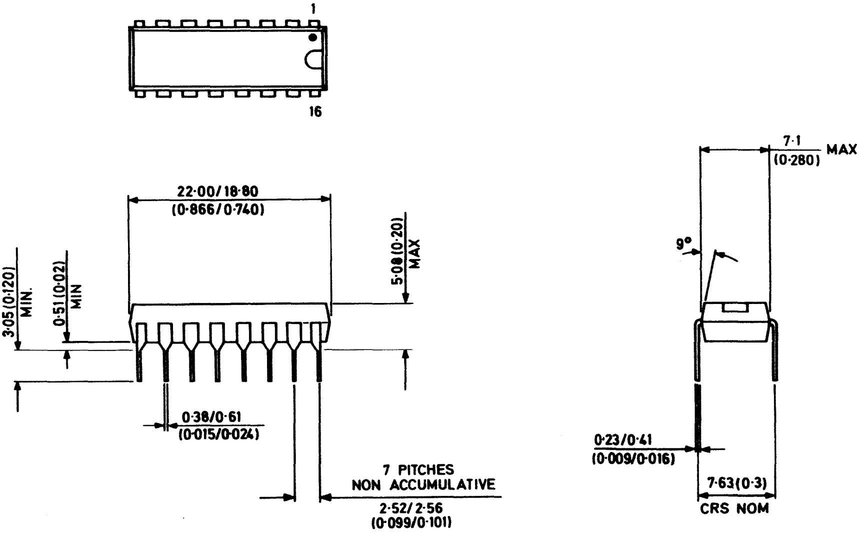

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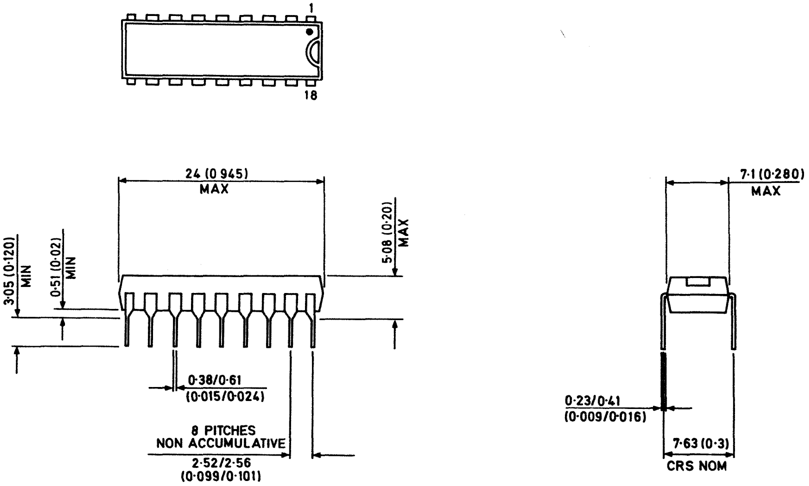
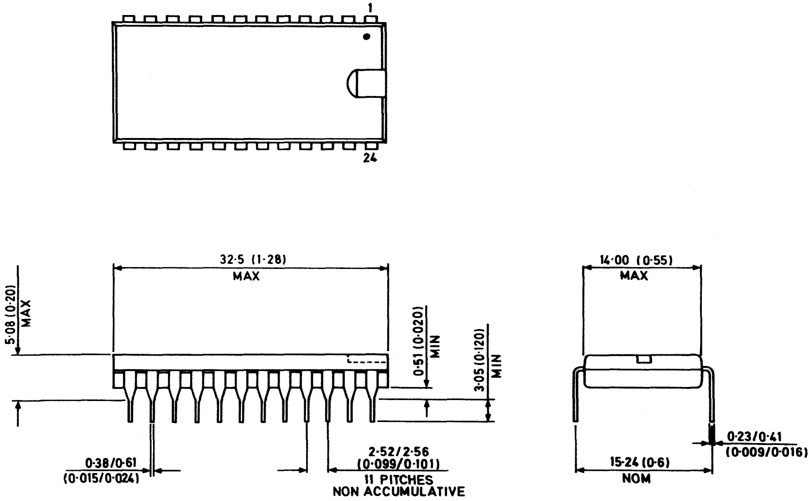


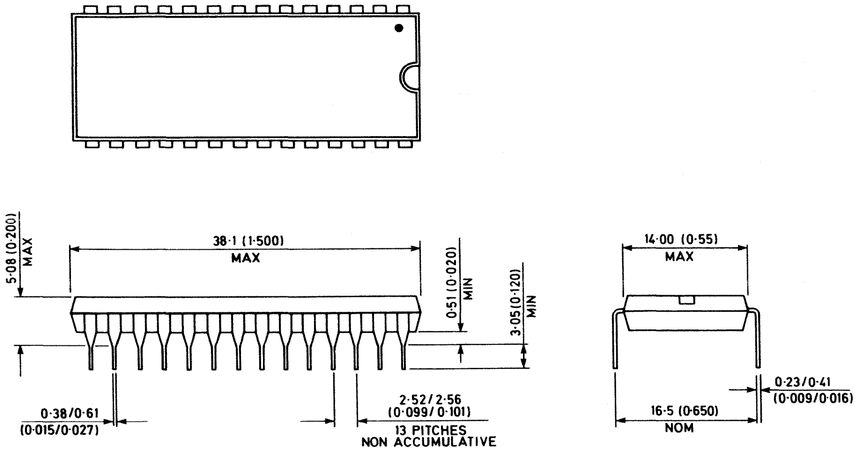
18 LEAD PLASTIC DIL

DP18



24 LEAD PLASTIC DIL

DP24



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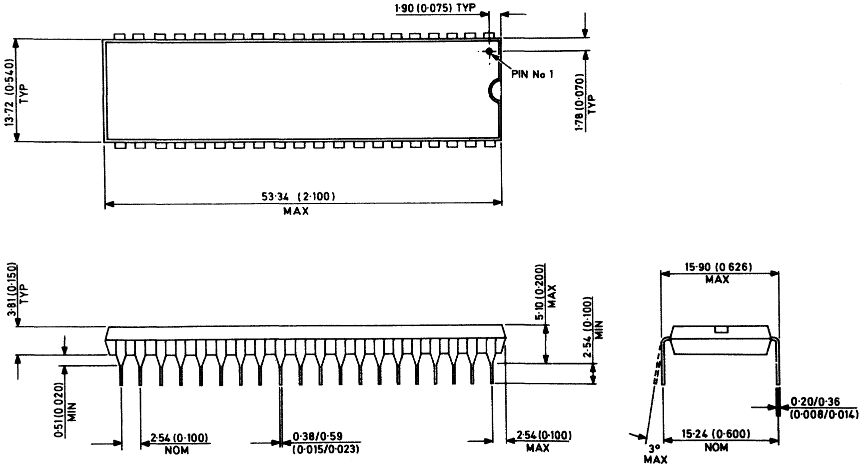

40 LEAD PLASTIC DIL **DP40**

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